Attacking the Red Brick Walls of the International Technology Roadmap for Semiconductors (ITRS)

Dr. Paolo Gargini

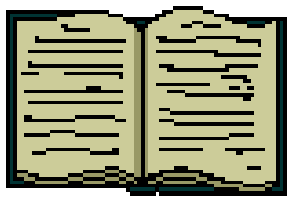
Chairman ITRS

M2 S2

Sept-23--2002

What is the ITRS?

- A consensus reference document with a 15 year outlook on the requirements of the semiconductor industry
  - Provides a ***reference*** document for Equipment, Materials and Software ***Suppliers*** on the ***Needs*** of the Semiconductor Industry and on ***Possible Solutions***
  - Provides a ***reference*** document for the ***researchers*** on the challenges of the semiconductor industry in the out years



Technology Hierarchy

Example:

- **Technology Needs**
- **Metal Potential Solution: Cu Metal**
- **Dielectric Potential Solution: Low K**
- **Use: Cu CVD Seed Layer + Cu Plating+ CMP+Low K CVD**
- **Establish Supplier Infrastructure**

Technology Roadmap Domain

Technology Implementation Domain

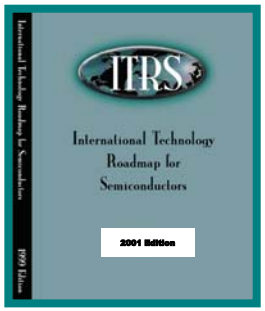
duce Signal Propagation Delay of
rconnections

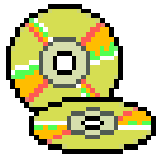
ions

Det
lentation

Roadmap Editions

http://public.itrs.net





1991
Micro Tech 2000
Workshop Report

1992NTRS

1994NTRS

1997NTRS

1998ITRS
Update

1999ITRS

2000ITRS
Update

2001ITRS

2002ITRS
Update

Europe

Japan

Korea

Taiwan

USA

ITRS

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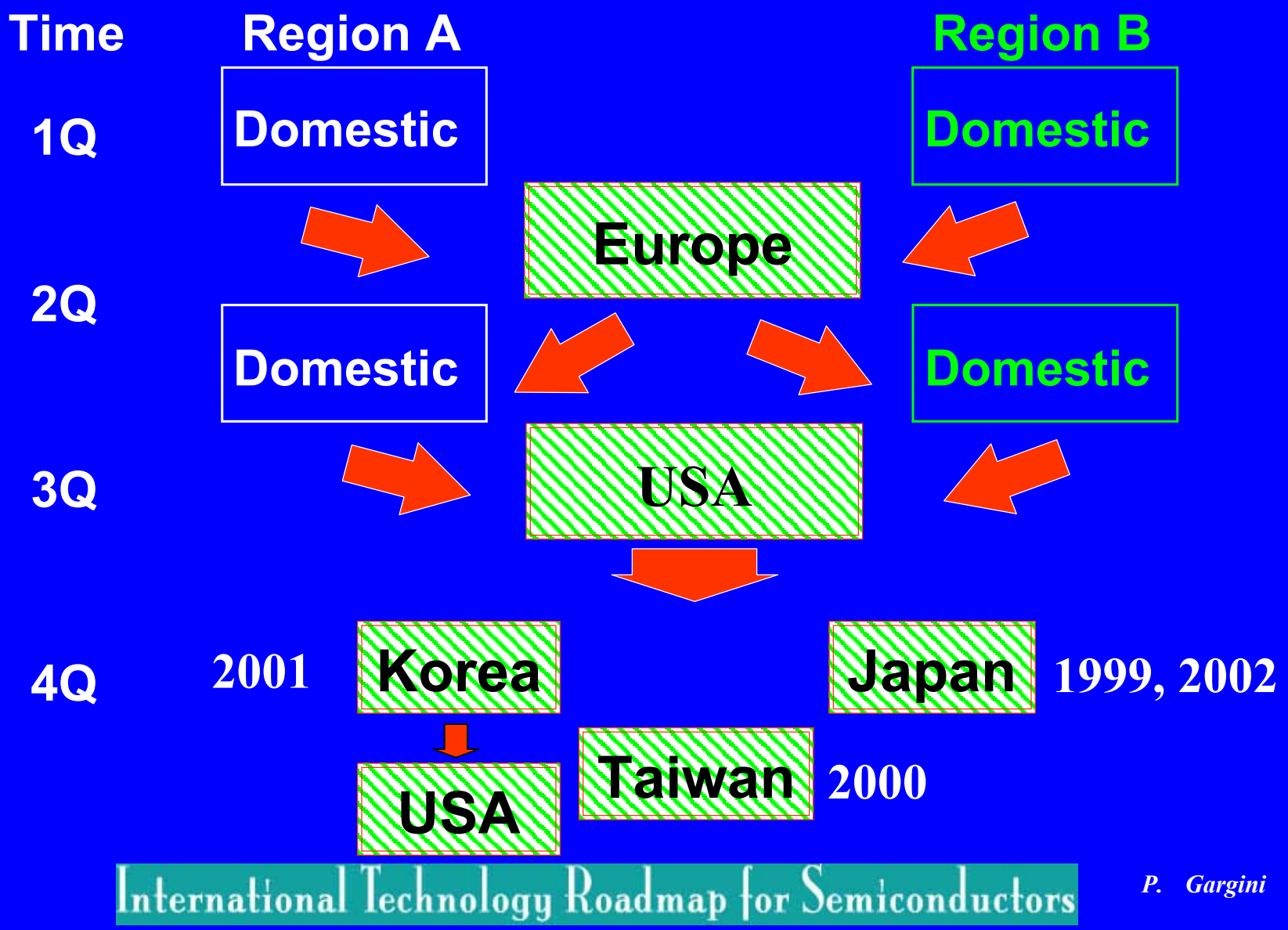
International and Domestic Timing



International Technology Roadmap for Semiconductors

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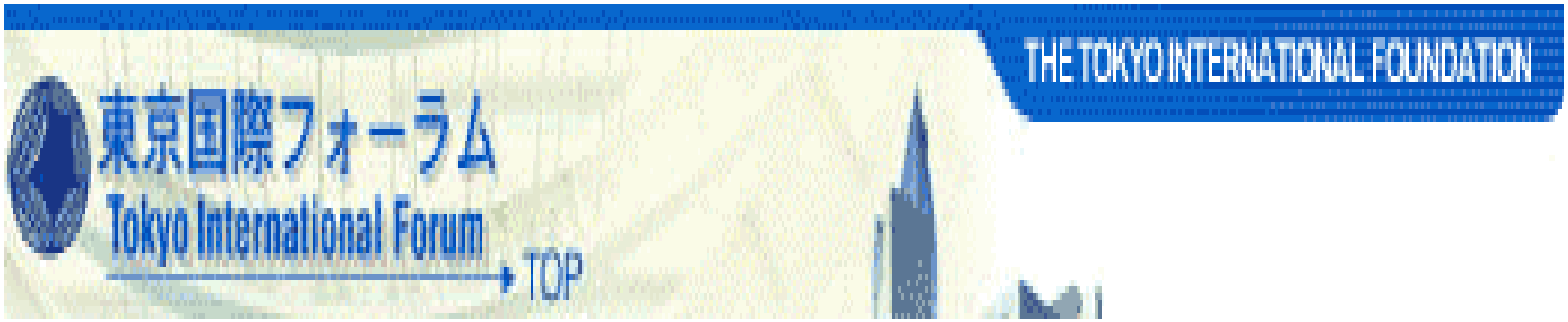
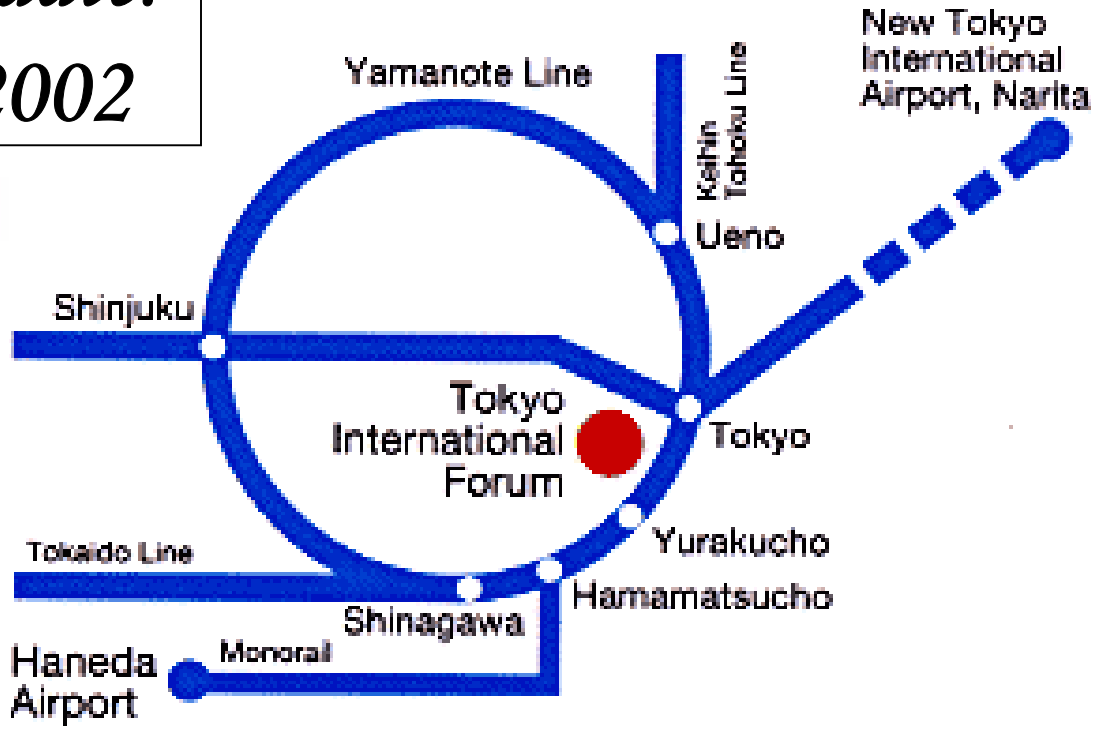
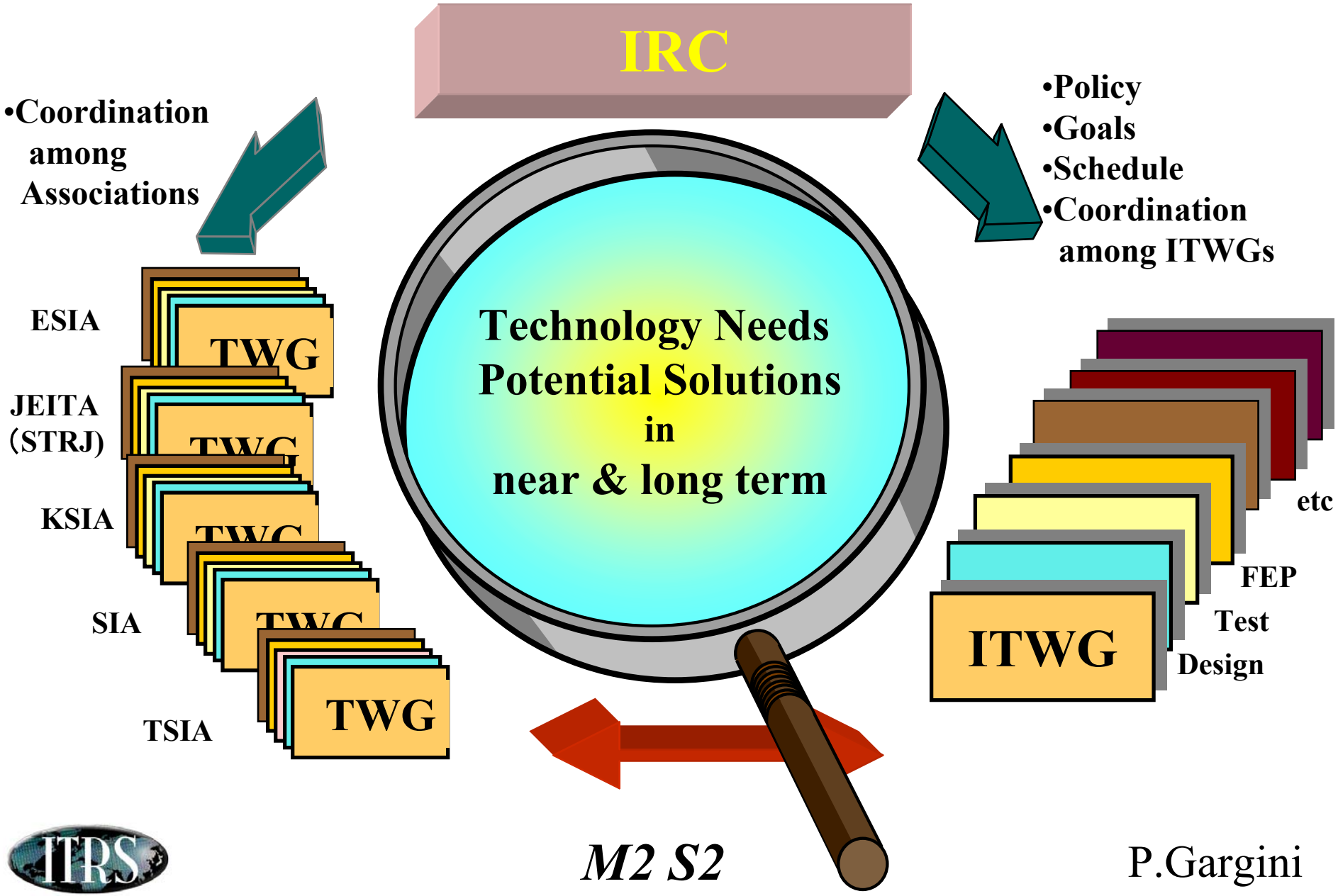


2002 ITRS Update: December 4th, 2002



Mission of ITRS



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International Technology Working Groups

ITWG

- Assembly & Packaging
- Design
- Factory Integration
- Front End Process
- Interconnect
- Lithography
- PIDS, Emerging Devices
- Test

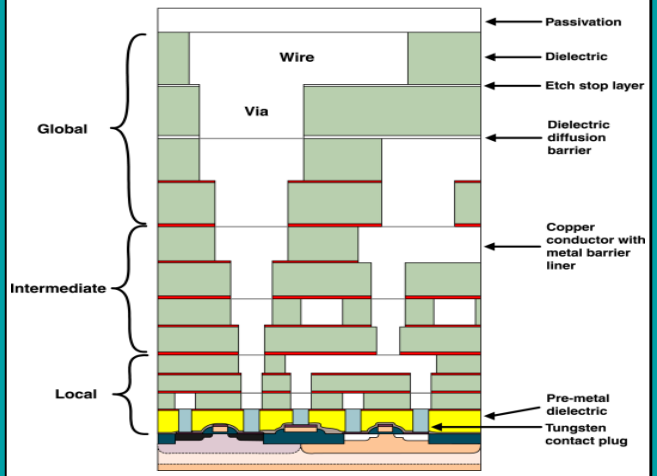
Cross ITWG

- Environment, Safety, Health
- Metrology
- Modeling and Simulation
- Yield Enhancement

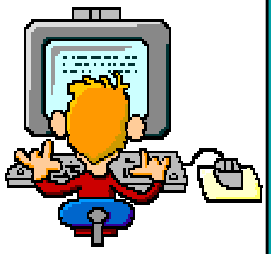
* PIDS=Process Integration and Device Structures

ITRS Framework

Interconnect

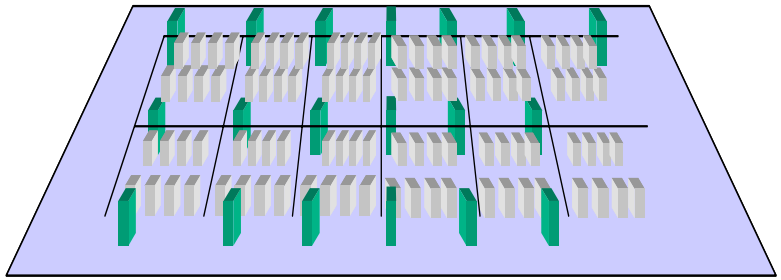


Design



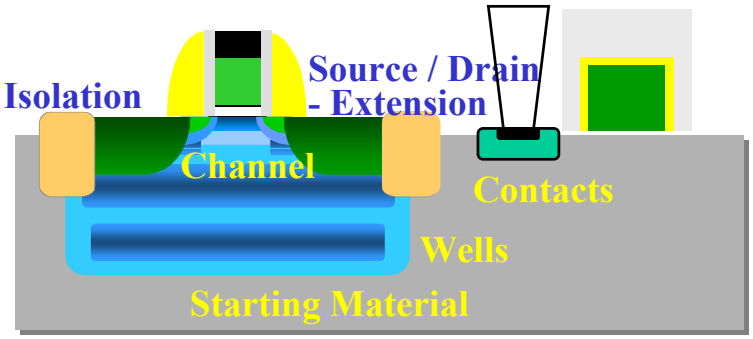
ESH

Factory Integration

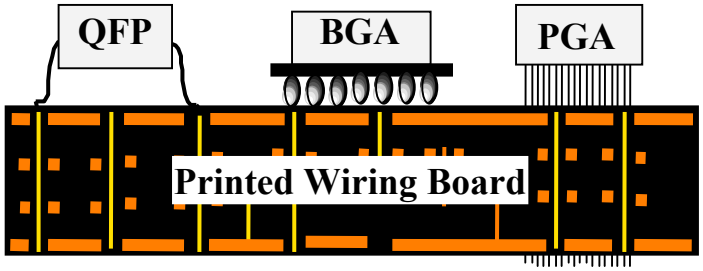


Yield Enhancement

Metrology Modeling Lithography PIDS FEP

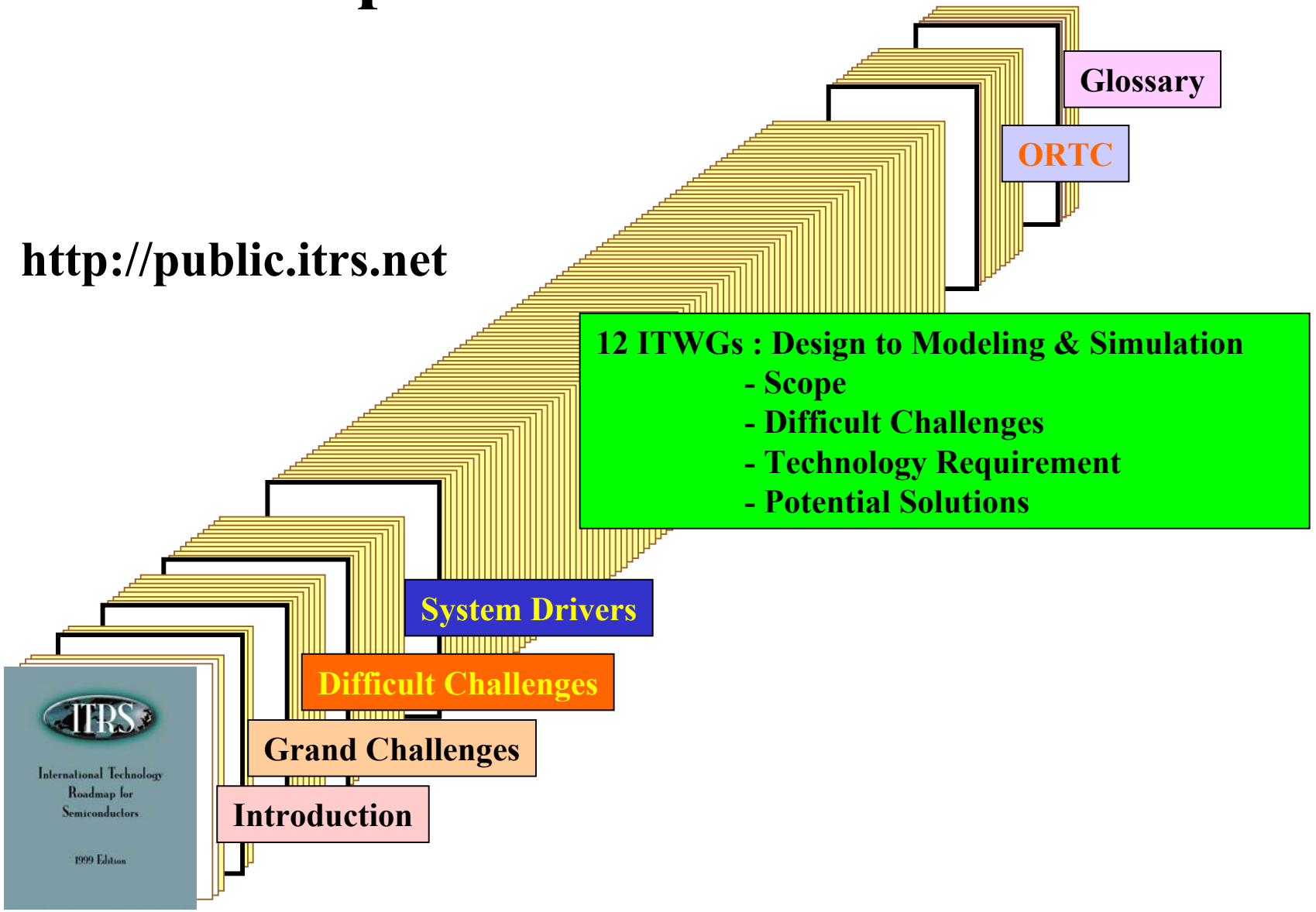


Assembly Test



Chapters of ITRS 2001

http://public.itrs.net



Contact Information for the ITRS

- **For general questions or information regarding ITRS publications and public forums visit the ITRS web site http://public.itrs.net [*note that there is no "www" in our web site address*.].**
  To order a Roadmap through email, use the ITRS email address technology.roadmap@sematech.org or access the ITRS web site.

- **Other questions or comments?**

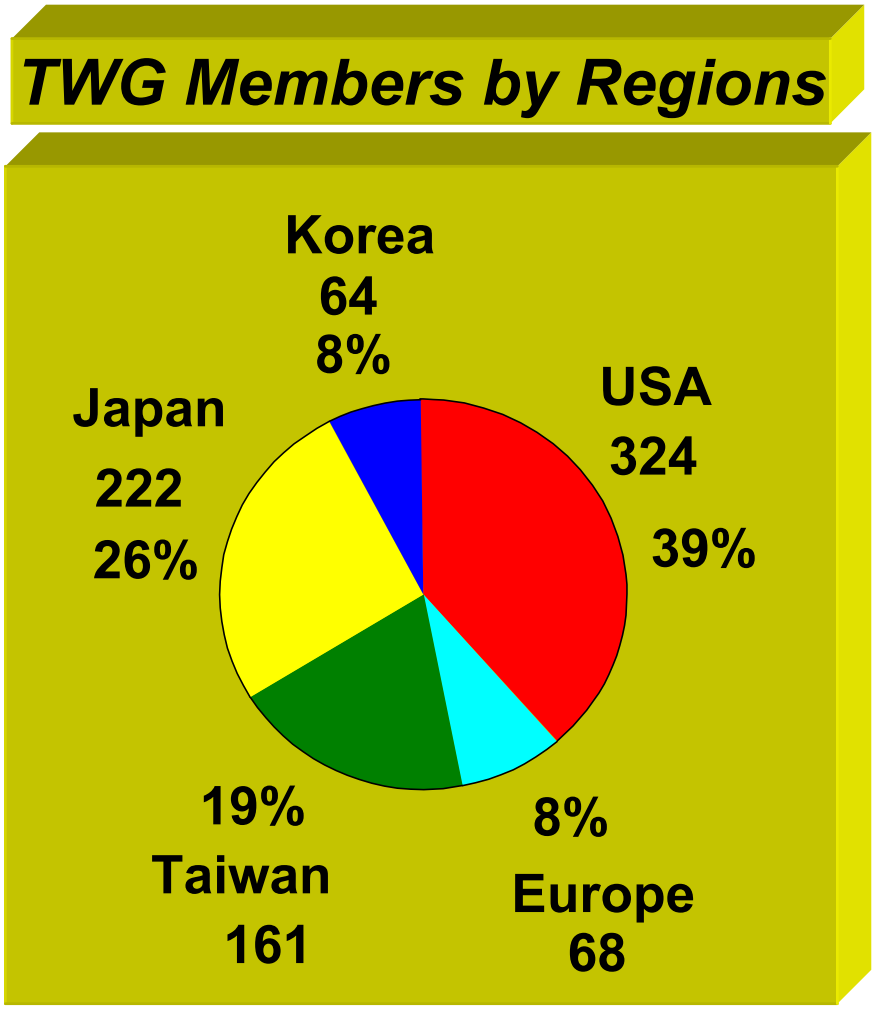
call
Linda Wilson
ITRS Information Manager
512.356.3605

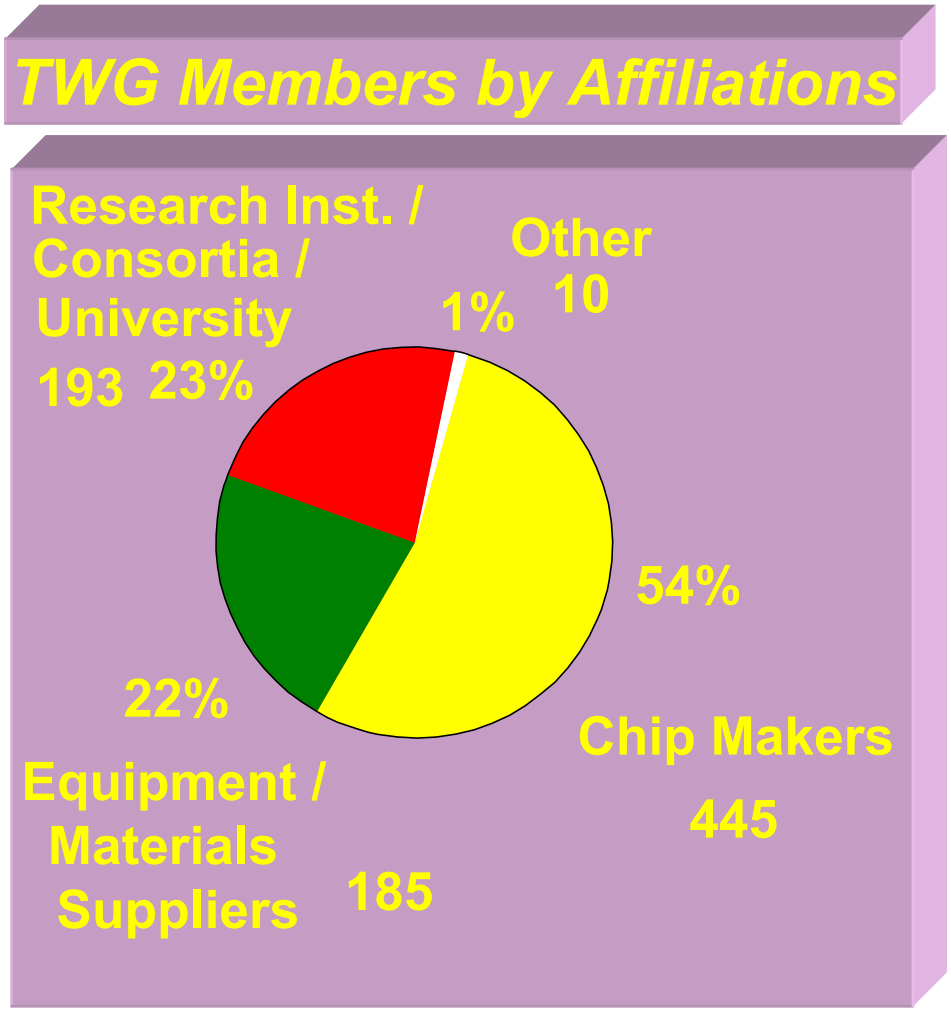
Sarah Mangum
ITRS Webmaster
512.356.3558

2001 ITRS Book and CD sales

- **$25 for CDs, $35 for CDs shipped outside the U.S.A**
- **$50 for Books, $65 for ITRS books shipped outside the U.S.A.**
- ***Back issues of the ITRS are available while quantities last (1999, 1997, 1994) !!***

Composition of the Technology Working Group (ITWG) in 2001





Applied Materials
KLA-Tencor
Tokyo Electron America
SEMI
Novellus Systems
Wacker Siltronic Corp.
Agilent Technologies
Winbond Electronics Corp.
Axcelis Technologies, Inc.
Komatsu Silicon
MEMC
Canon Inc.

DuPont Company
Silicon Valley Group, Inc
ION Systems
M+W Zandar
Nanya Technology Co.
Compaq Computer Corp
Asyst Technologies, Inc.
Sumitomo Sitix Corp.
Varian
Air Products & Chemicals
Etec Systems, Inc.
n-Line Corporation
K&S

CamLine
Ebara
Rohm
Sanyo
FSI International
Genus
Ibis Technology
Okmetic Ltd.
SiGen
Soitec
Tokin Corp
BOC Edwards

THANK YOU!!!

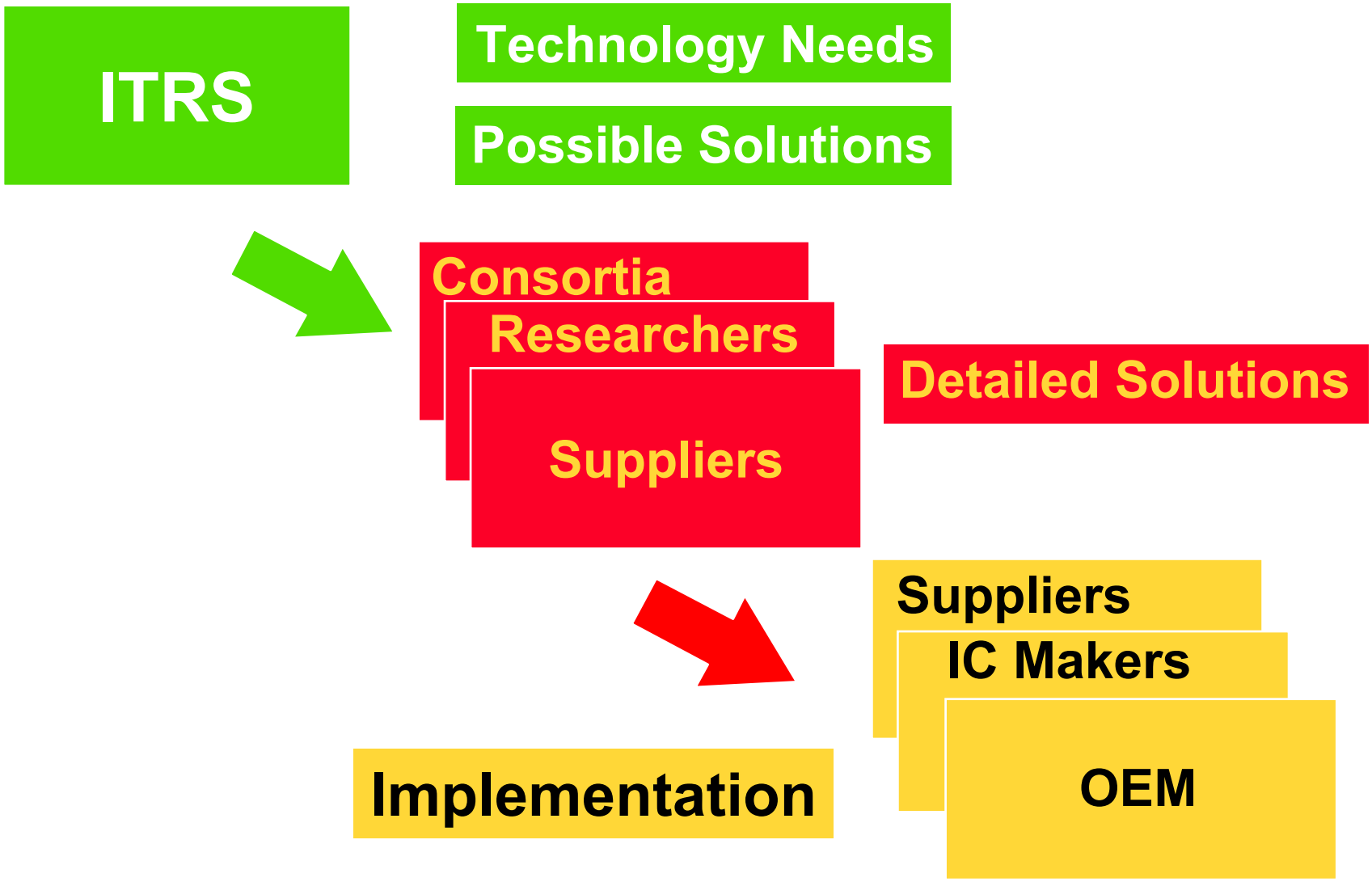
Dow Chemical
Micronix
ASM Lithography
Nikon Corporation
Photronics, Inc.
Shipley Company, Inc.
Episil Technologies
Metrology Edge
Therma-Wave
Oki Electric Ind. Co., Ltd.

Advantest
LogicVision
Teradyne
Air Liquide
Metara, Inc.
Millipore

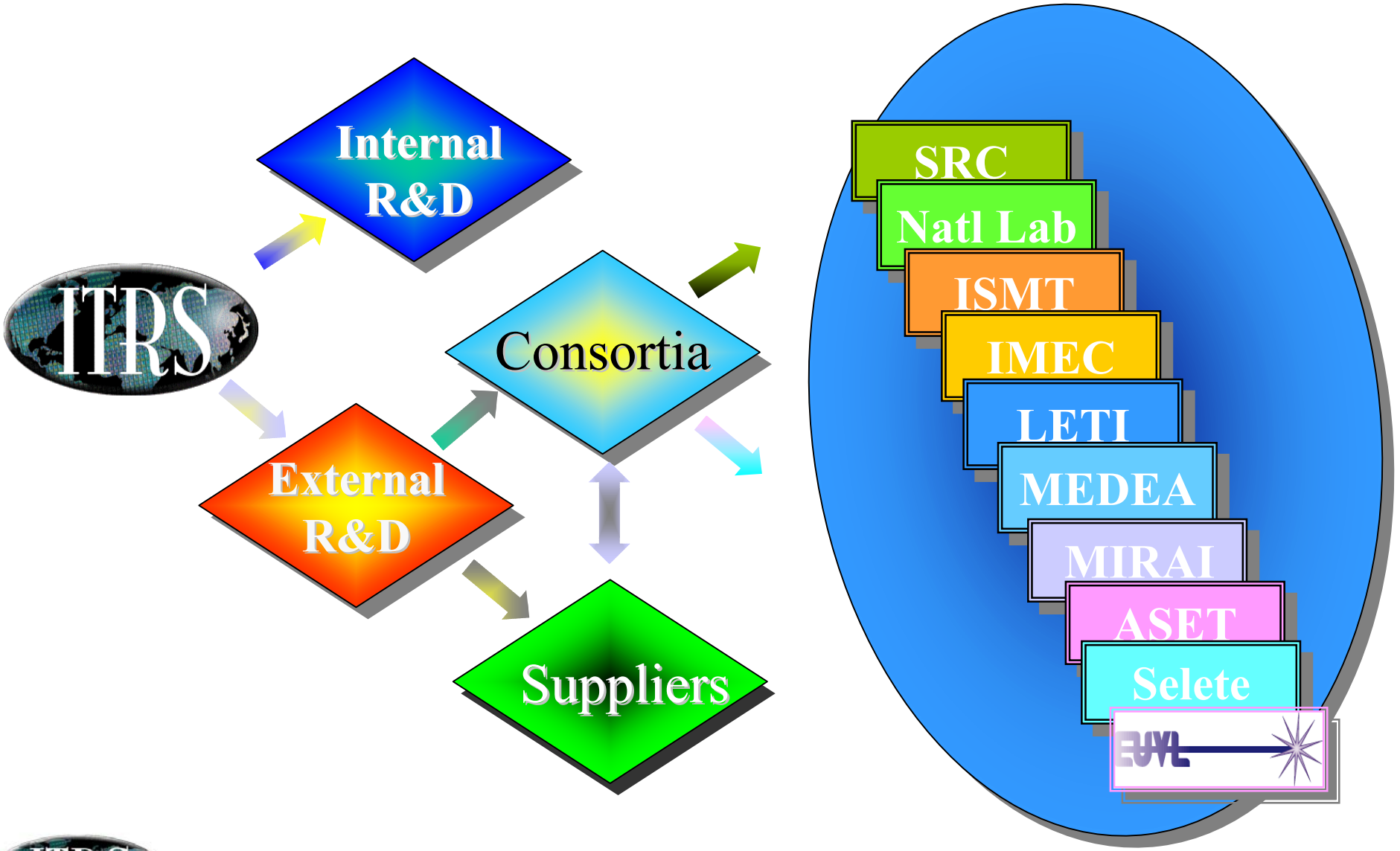
Nortel Networks
Cadence
Intransa
UBC
ATMI
Cabot Corporation
E4 Technologies
Praxair, Inc.
SONY
URS Corporation

DETAILED SOLUTIONS
And
IMPLEMENTATION

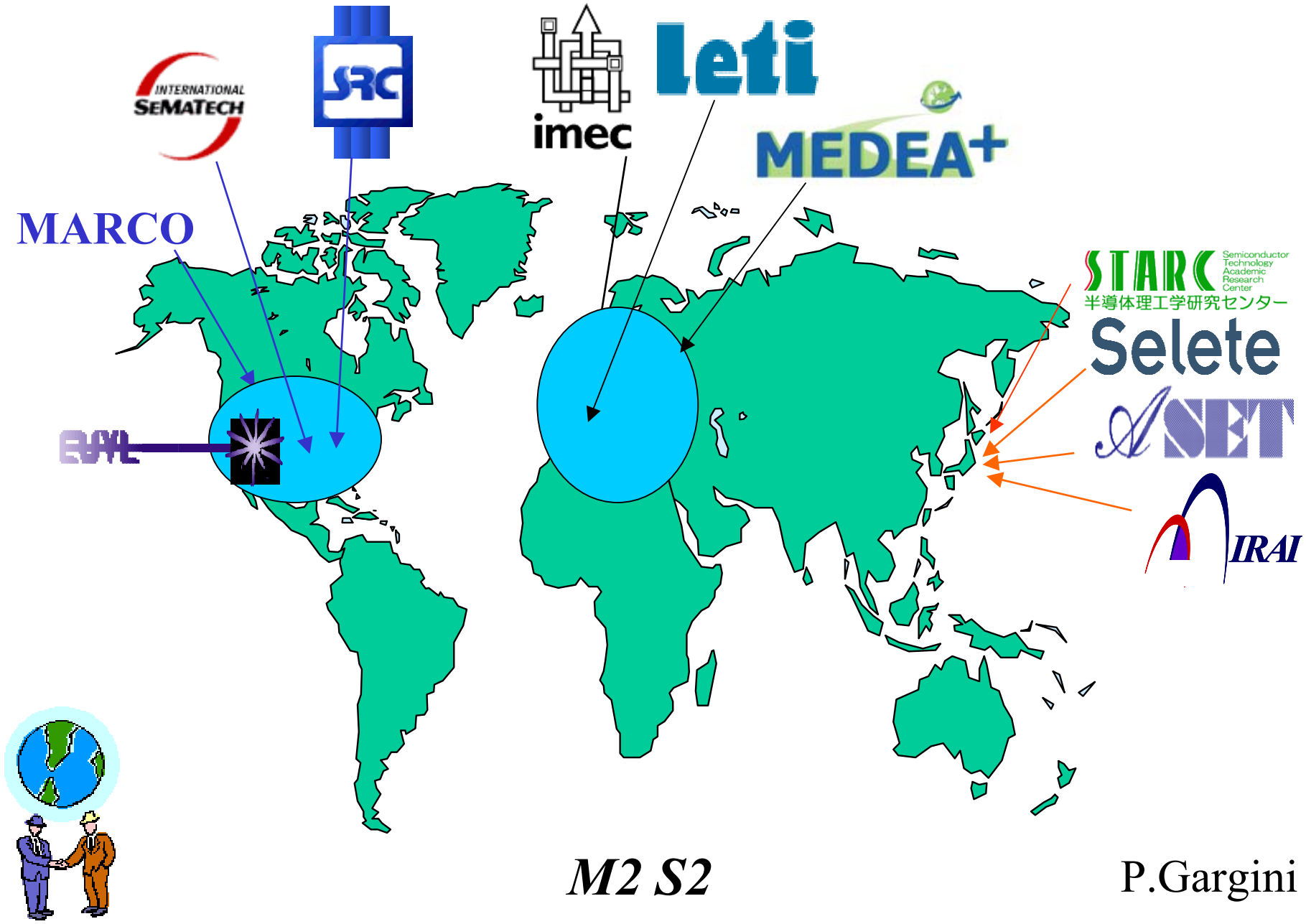
From Strategy to Implementation



Use of ITRS as a Global Planning Tool



Consortia Locations



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hiko Takamori

International Consortia Cooperation Initiative

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SRC

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SEMATECH

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one

Internet

ITRS GUIDING PRINCIPLE

M2 S2

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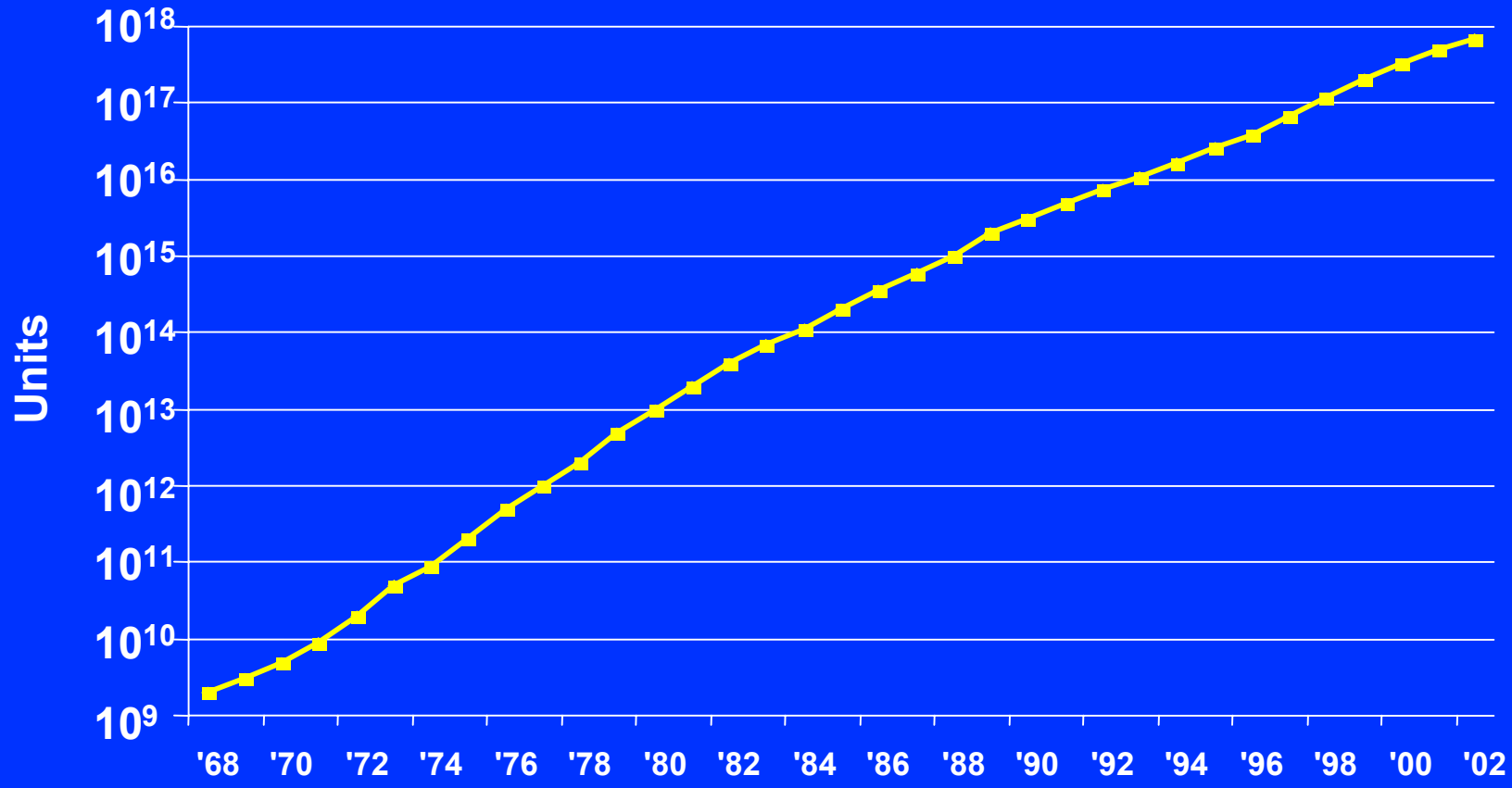
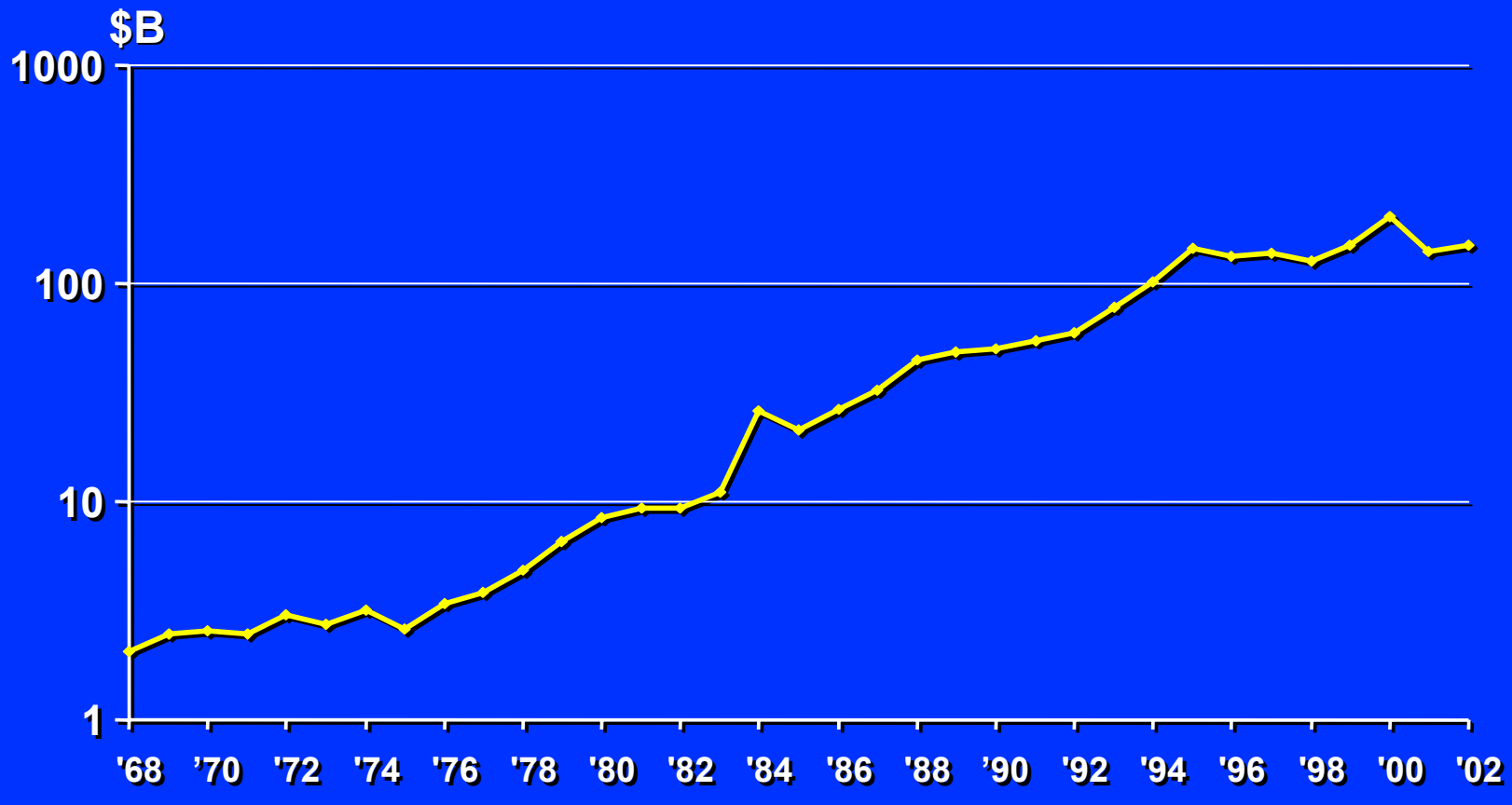
Transistors Shipped per Year



Source: WSTS/Dataquest/Intel, 8/02

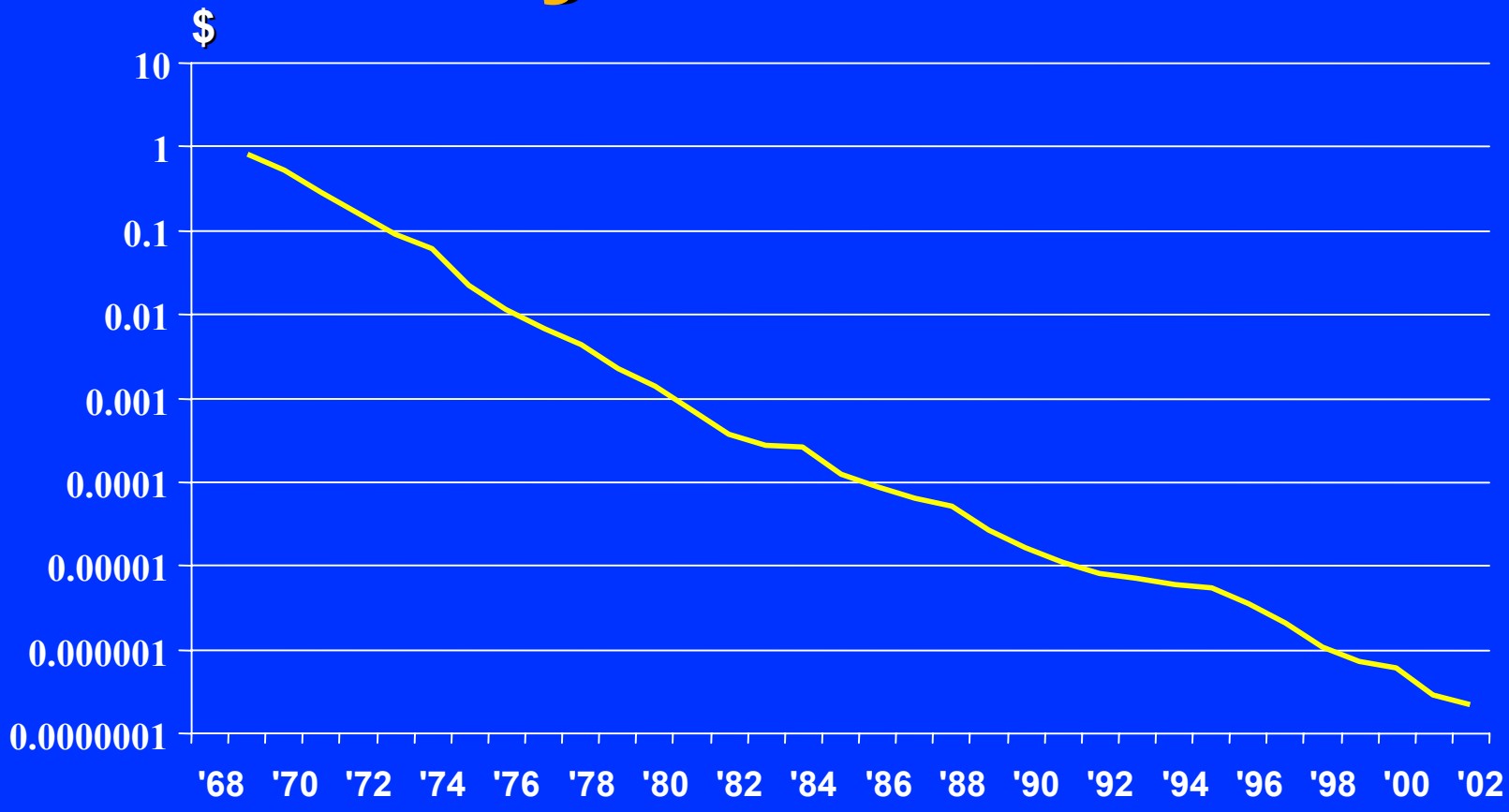
Worldwide Semiconductor Revenues



Source: Intel/WSTS, 8/02

intel

Average Transistor Price by Year



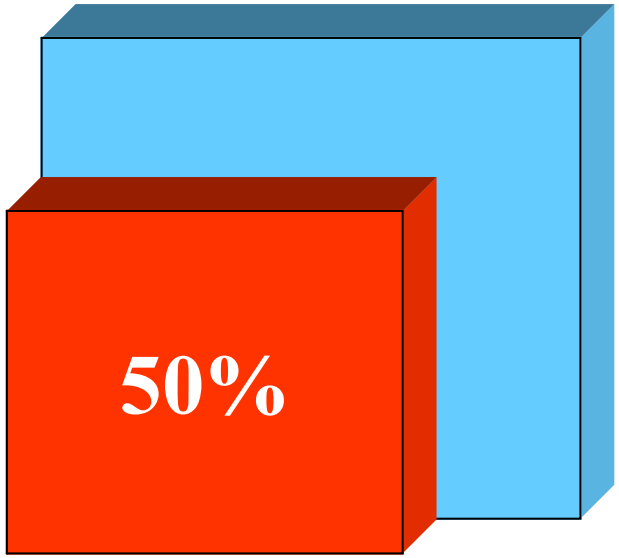
Source: WSTS/Dataquest/Intel, 8/02

®

ITRS GUIDING PRINCIPLE

50% TRANSISTOR AREA READUCION GENERATION TO GENERATION

=> 30% LINEAR FEATURE REDUCTION



Intel's Process Technology

Basic Feature Size in microns

0.8µ 0.6µ 0.35µ 0.25µ 0.18µ 0.13µ

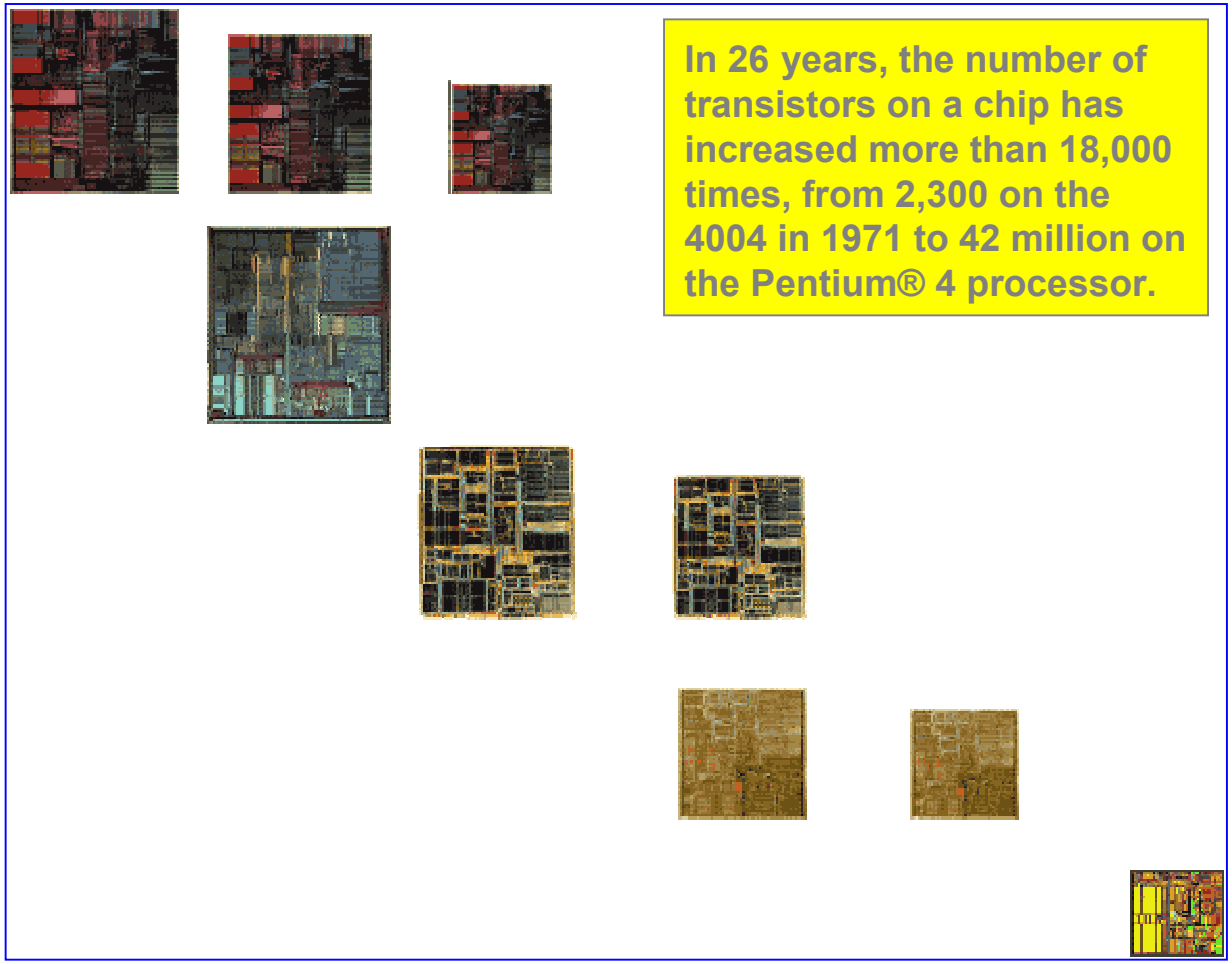
Pentium® Processor

Pentium® Pro Processor

Pentium® II Processor

Pentium® III Processor

Pentium® 4 Processor



In 26 years, the number of transistors on a chip has increased more than 18,000 times, from 2,300 on the 4004 in 1971 to 42 million on the Pentium® 4 processor.

DEFINITIONS
And
TIMING

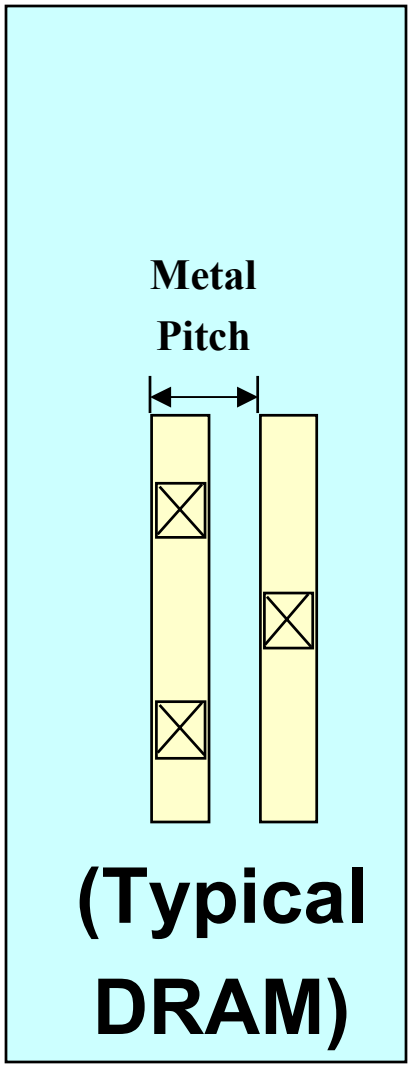
Technology Node Definition

One half of the smallest pitch in the technology,

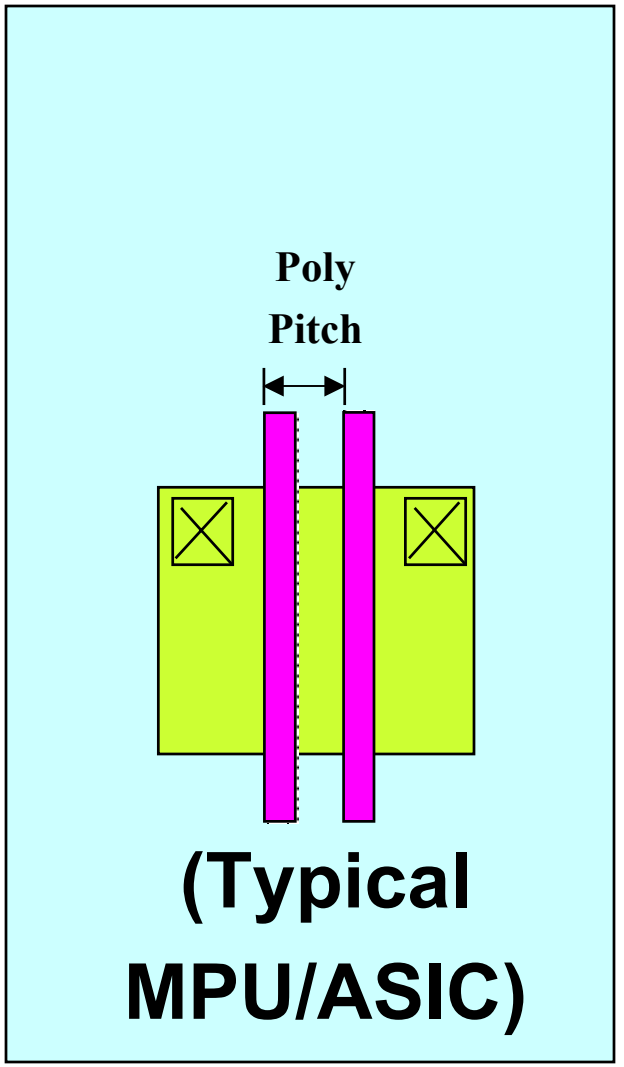
Typically represented by the first metal layer

of DRAM

Half Pitch (=Pitch/2) Definition



(Typical DRAM)



(Typical MPU/ASIC)

MOS Transistor Scaling
(1974 to present)

S=0.7

[0.5x per 2 nodes]

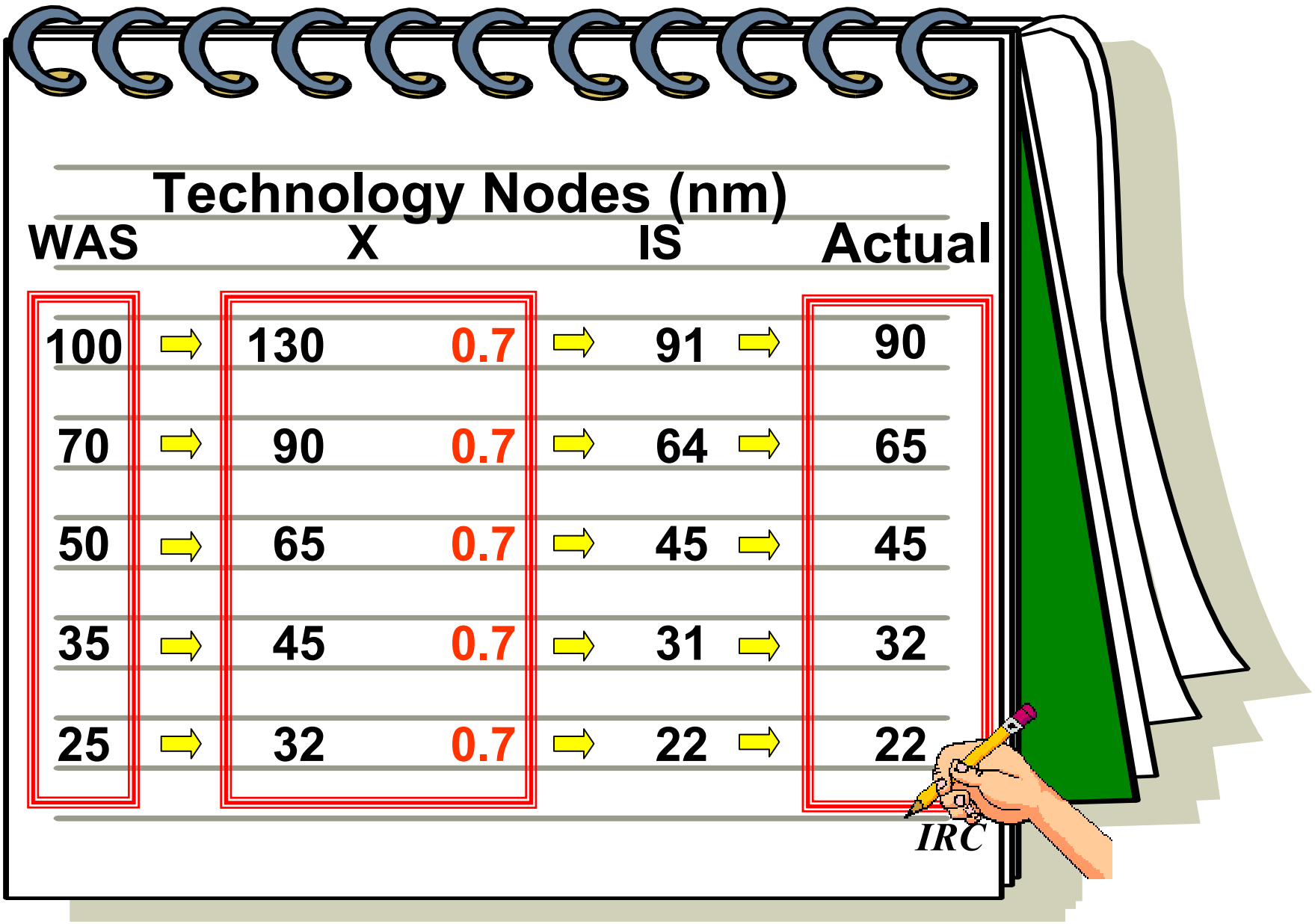
1994 NTRS Roadmap

Year:	95	96	97	98	99	00	01	02	03	04	05	06	07
NTRS'94	●			●			●			●			●
1/2 pitch*	350			250			180			130			100

* Dimensions for minimum half pitch and isolated line in nm

Source: National Technology Roadmap for Semiconductors

Back to Basics


Technology Nodes (nm)
WAS
X
IS
Actual
100 130 0.7 91 90
70 90 0.7 64 65
50 65 0.7 45 45
35 45 0.7 31 32
25 32 0.7 22 22
IRC

1999 ITRS Timing

Year of Production	1999 180	2000	2001	2002 130	2003	2004	2005 100
DRAM ½ Pitch (nm)	180	165	150	130	120	110	100
MPU Gate Length (nm)	140	120	100	85-90	80	70	65
MPU / ASIC ½ Pitch (nm)	230	210	180	160	145	130	115
ASIC Gate Length (nm)	180	165	150	130	120	110	100

2001 ITRS Timing

-1 -2 -2

Year of Production	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch	150	130	107	90	80	70	65
MPU Pr Gate Length	90	75	65	53	45	40	35
MPU Ph Gate Length -4	65	53	45	37	32	28	25

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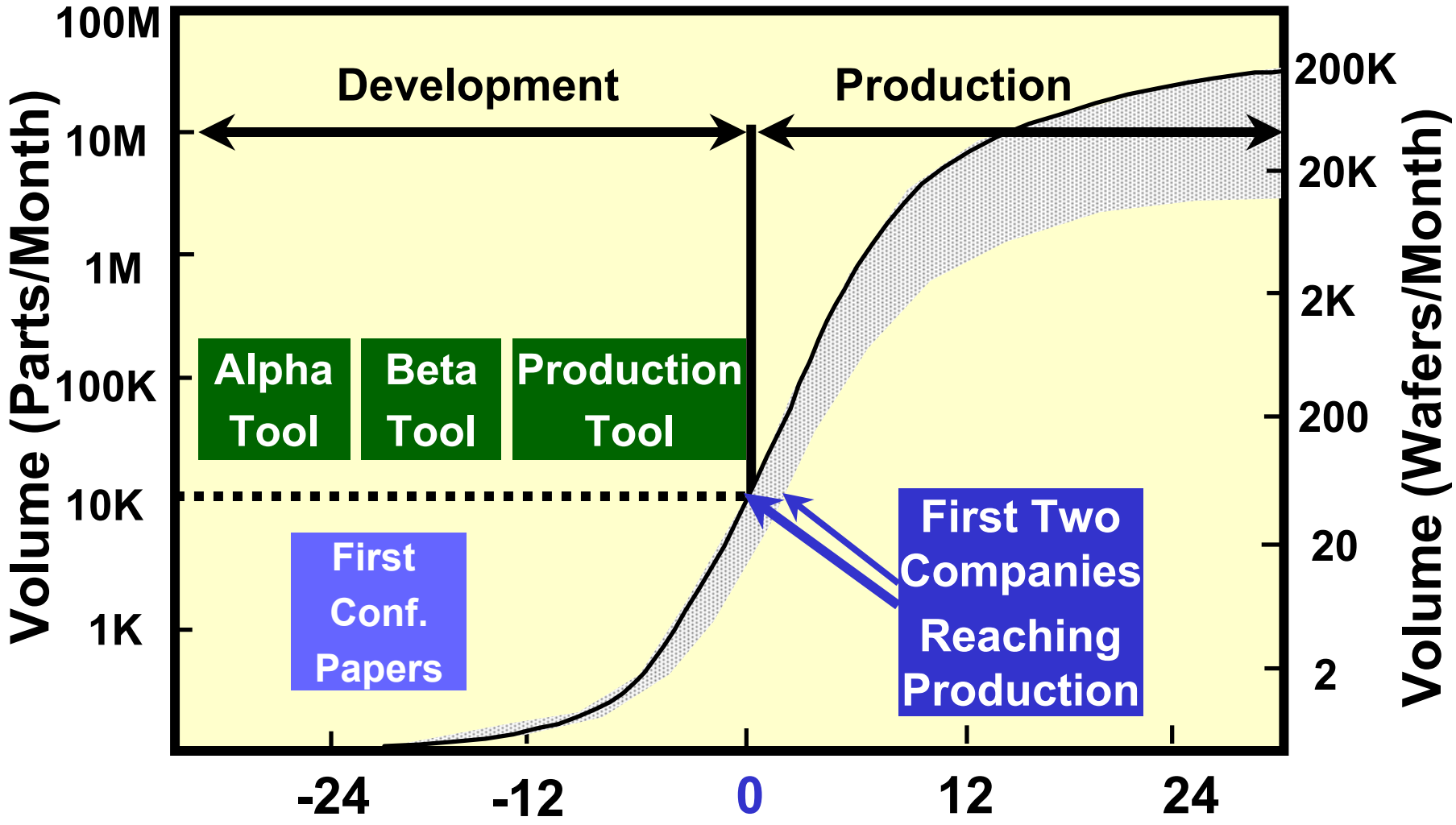
Production Ramp-up Model and Technology Node



Source: 2001 ITRS - Exec. Summary

3-year cycle (1977~1995)

Innovation 1.4X

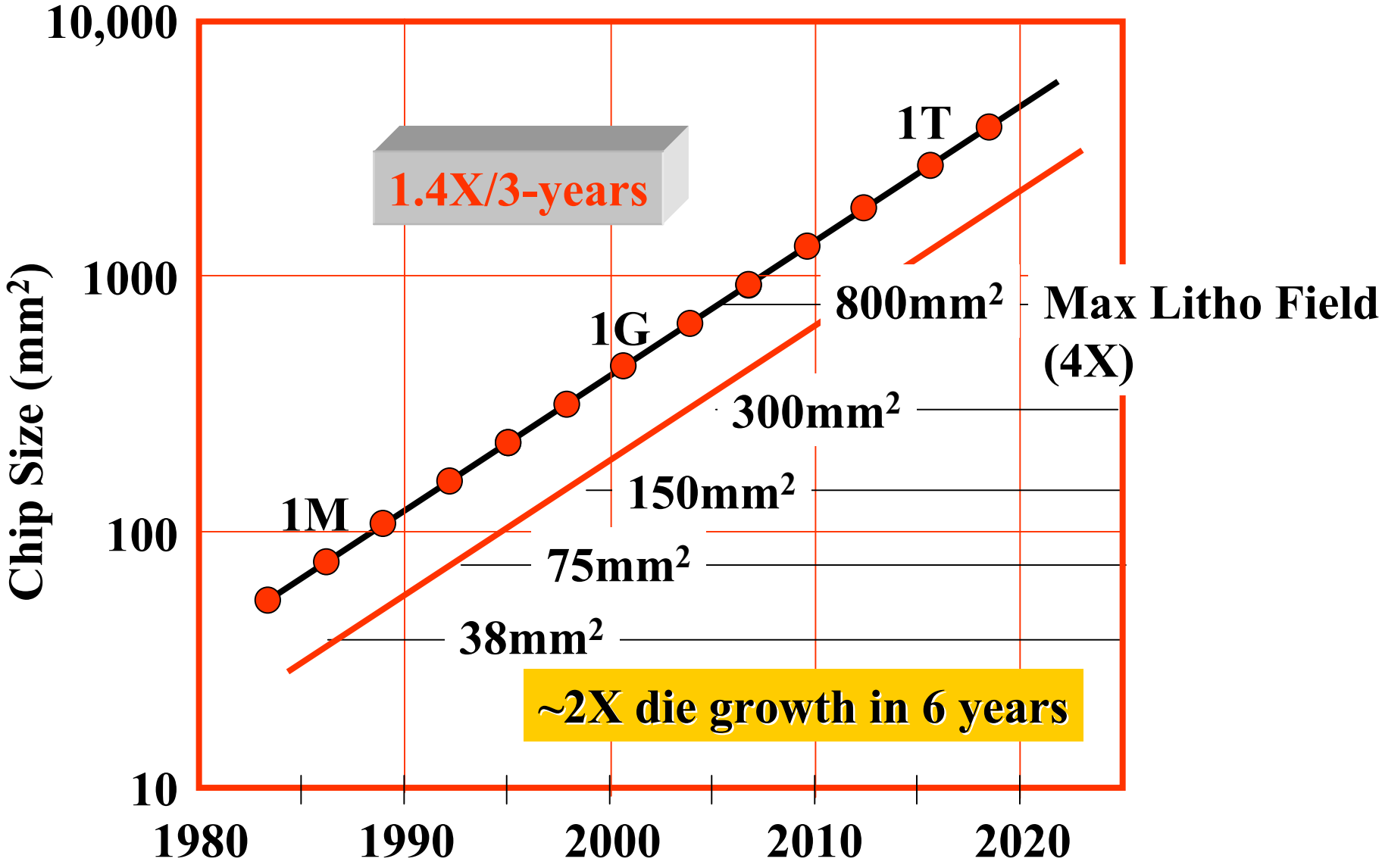
3-year cycle

4X/3 Years

Technology 2X

Manufacturing 1.4X

DRAM Chip Size Trend



3-year -> 2-year cycle (~1995-2010)

Innovation

1.4X

3-year cycle

4X/3 Years

Technology

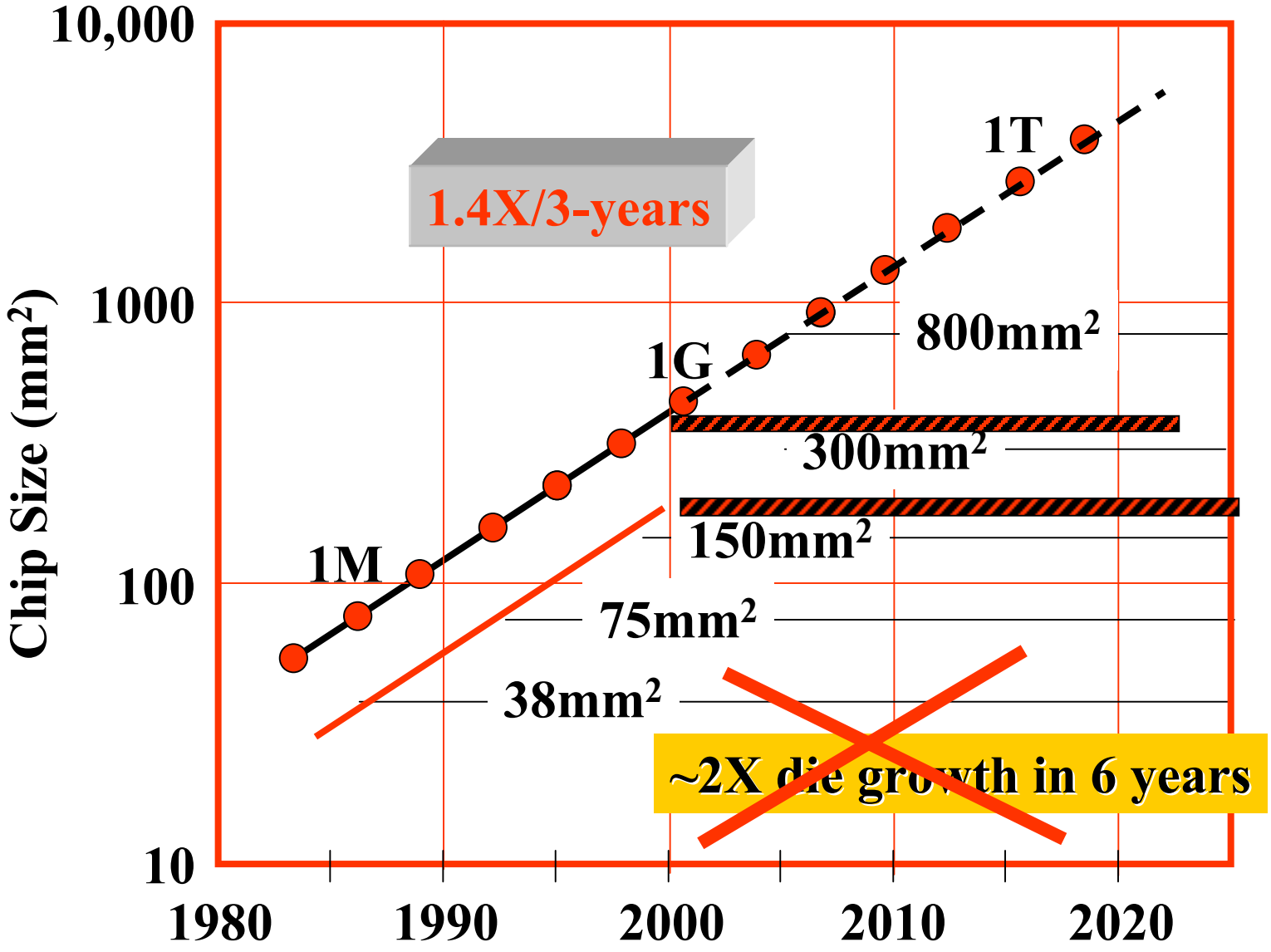
2X->2.8X

Manufacturing

1.4X->1.0X

1.4X

DRAM Chip Size Trend



TABLES
And
WALLS

Table's Structure

- All tables are divided in two parts:
  - **Near Term**
    - Six year outlook (e.g., 2001-2007)
    - All values are reported on a yearly basis
  - **Long Term**
    - Nine year outlook (e.g., 2008-2016)
    - Values are reported at 3 year interval

Tables' Color Scheme

Solutions Exist

White

Solutions Being Pursued

Yellow

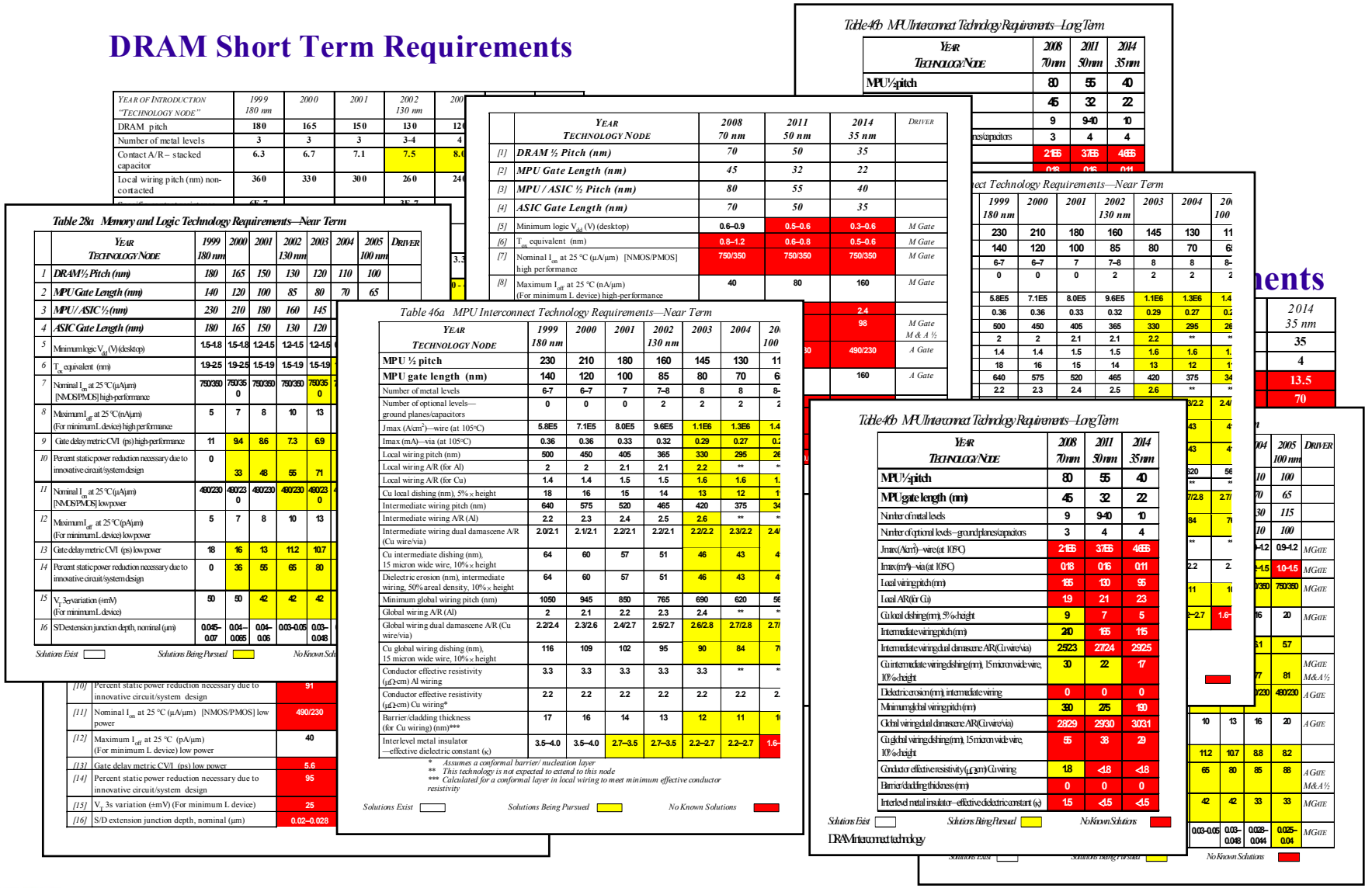
No Known Solutions

Red

- A new category will be introduced starting with 2002ITRS Update

A Rainbow of Tables

DRAM Short Term Requirements



Year of Introduction "Technology Node"	1999 180 nm	2000	2001	2002 130 nm	200
DRAM pitch	180	165	150	130	120
Number of metal levels	3	3	3	3-4	4
Contact A/R – stacked capacitor	6.3	6.7	7.1	7.5	8.0
Local wiring pitch (nm) non-contacted	360	330	300	260	240

Table 28a Memory and Logic Technology Requirements—Near Term

	Year / Technology Node	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	Driver
1	DRAM ½ Pitch (nm)	180	165	150	130	120	110	100	
2	MPU Gate Length (nm)	140	120	100	85	80	70	65	
3	MPU / ASIC ½ (nm)	230	210	180	160	145			
4	ASIC Gate Length (nm)	180	165	150	130	120			
5	Minimum logic V_{dd} (V) (desktop)	1.5-1.8	1.5-1.8	1.2-1.5	1.2-1.5	1.2-1.5			
6	T_{ox} equivalent (nm)	1.9-2.5	1.9-2.5	1.5-1.9	1.5-1.9	1.5-1.9			
7	Nominal I_{on} at 25 °C (µA/µm) [NMOS/PMOS] high-performance	750/350	750/350	750/350	750/350	750/350			
8	Maximum I_{off} at 25 °C (nA/µm) (For minimum L device) high performance	5	7	8	10	13			
9	Gate delay metric CV/I (ps) high-performance	11	9.4	8.6	7.3	6.9			
10	Percent static power reduction necessary due to innovative circuit/system design	0		33	48	55	71		
11	Nominal I_{on} at 25 °C (µA/µm) [NMOS/PMOS] low power	480/230	480/230	480/230	480/230	480/230			
12	Maximum I_{off} at 25 °C (pA/µm) (For minimum L device) low power	5	7	8	10	13			
13	Gate delay metric CV/I (ps) low power	18	16	13	11.2	10.7			
14	Percent static power reduction necessary due to innovative circuit/system design	0	36	55	65	80			
15	V_T 3σ variation (±mV) (For minimum L device)	50	50	42	42	42			
16	S/D extension junction depth, nominal (µm)	0.045-0.07	0.04-0.065	0.04-0.05	0.03-0.05	0.03-0.048			

Solutions Exist | Solutions Being Pursued | No Known Solutions

	Year / Technology Node	2008 70 nm	2011 50 nm	2014 35 nm	Driver
[1]	DRAM ½ Pitch (nm)	70	50	35	
[2]	MPU Gate Length (nm)	45	32	22	
[3]	MPU / ASIC ½ Pitch (nm)	80	55	40	
[4]	ASIC Gate Length (nm)	70	50	35	
[5]	Minimum logic V_{dd} (V) (desktop)	0.6–0.9	0.5–0.6	0.3–0.6	M Gate
[6]	T_{ox} equivalent (nm)	0.8–1.2	0.6–0.8	0.5–0.6	M Gate
[7]	Nominal I_{on} at 25 °C (µA/µm) [NMOS/PMOS] high performance	750/350	750/350	750/350	M Gate
[8]	Maximum I_{off} at 25 °C (nA/µm) (For minimum L device) high-performance	40	80	160	M Gate
[9]	Gate delay metric CV/I (ps) high-performance			2.4	
[10]	Percent static power reduction necessary due to innovative circuit/system design			98	M Gate M & A ½
[11]	Nominal I_{on} at 25 °C (µA/µm) [NMOS/PMOS] low power			490/230	A Gate
[12]	Maximum I_{off} at 25 °C (pA/µm) (For minimum L device) low power			160	A Gate
[13]	Gate delay metric CV/I (ps) low power				
[14]	Percent static power reduction necessary due to innovative circuit/system design				
[15]	V_T 3s variation (±mV) (For minimum L device)				
[16]	S/D extension junction depth, nominal (µm)				

Table 46a MPU Interconnect Technology Requirements—Near Term

Year / Technology Node	1999 180 nm	2000	2001	2002 130 nm	2003	2004	20 100
MPU ½ pitch	230	210	180	160	145	130	11
MPU gate length (nm)	140	120	100	85	80	70	6
Number of metal levels	6-7	6–7	7	7–8	8	8	8-
Number of optional levels—ground planes/capacitors	0	0	0	2	2	2	2
Jmax (A/cm²)—wire (at 105°C)	5.8E5	7.1E5	8.0E5	9.6E5	1.1E6	1.3E6	1.4
Imax (mA)—via (at 105°C)	0.36	0.36	0.33	0.32	0.29	0.27	0.2
Local wiring pitch (nm)	500	450	405	365	330	295	26
Local wiring A/R (for Al)	2	2	2.1	2.1	2.2	**	**
Local wiring A/R (for Cu)	1.4	1.4	1.5	1.5	1.6	1.6	1.
Cu local dishing (nm), 5% × height	18	16	15	14	13	12	1
Intermediate wiring pitch (nm)	640	575	520	465	420	375	34
Intermediate wiring A/R (Al)	2.2	2.3	2.4	2.5	2.6	**	**
Intermediate wiring dual damascene A/R (Cu wire/via)	2.0/2.1	2.1/2.1	2.2/2.1	2.2/2.1	2.2/2.2	2.3/2.2	2.4/
Cu intermediate dishing (nm), 15 micron wide wire, 10% × height	64	60	57	51	46	43	4
Dielectric erosion (nm), intermediate wiring, 50% areal density, 10% × height	64	60	57	51	46	43	4
Minimum global wiring pitch (nm)	1050	945	850	765	690	620	56
Global wiring A/R (Al)	2	2.1	2.2	2.3	2.4	**	**
Global wiring dual damascene A/R (Cu wire/via)	2.2/2.4	2.3/2.6	2.4/2.7	2.5/2.7	2.6/2.8	2.7/2.8	2.7/
Cu global wiring dishing (nm), 15 micron wide wire, 10% × height	116	109	102	95	90	84	7
Conductor effective resistivity (µΩ-cm) Al wiring	3.3	3.3	3.3	3.3	3.3	**	**
Conductor effective resistivity (µΩ-cm) Cu wiring*	2.2	2.2	2.2	2.2	2.2	2.2	2.
Barrier/cladding thickness (for Cu wiring) (nm)***	17	16	14	13	12	11	1
Interlevel metal insulator —effective dielectric constant (κ)	3.5–4.0	3.5–4.0	2.7–3.5	2.7–3.5	2.2–2.7	2.2–2.7	1.6–

* Assumes a conformal barrier/ nucleation layer
** This technology is not expected to extend to this node
*** Calculated for a conformal layer in local wiring to meet minimum effective conductor resistivity

Solutions Exist | Solutions Being Pursued | No Known Solutions

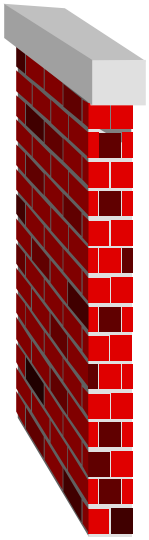
Table 46b MPU Interconnect Technology Requirements—Long Term

Year / Technology Node	2008 70 nm	2011 50 nm	2014 35 nm
MPU ½ pitch	80	55	40
MPU gate length (nm)	45	32	22
Number of metal levels	9	9-10	10
Number of optional levels—ground planes/capacitors	3	4	4
Jmax (A/cm²)—wire (at 105°C)	2.1E6	3.7E6	4.6E6
Imax (mA)—via (at 105°C)	0.18	0.16	0.11
Local wiring pitch (nm)	165	130	95
Local A/R (for Cu)	1.9	2.1	2.3
Cu local dishing (nm), 5% × height	9	7	5
Intermediate wiring pitch (nm)	240	185	115
Intermediate wiring dual damascene A/R (Cu wire/via)	2.5/2.3	2.7/2.4	2.9/2.5
Cu intermediate wiring dishing (nm), 15 micron wide wire, 10% × height	30	22	17
Dielectric erosion (nm), intermediate wiring	0	0	0
Minimum global wiring pitch (nm)	330	275	190
Global wiring dual damascene A/R (Cu wire/via)	2.8/2.9	2.9/3.0	3.0/3.1
Cu global wiring dishing (nm), 15 micron wide wire, 10% × height	55	38	29
Conductor effective resistivity (µΩ-cm) Cu wiring	1.8	<1.8	<1.8
Barrier/cladding thickness (nm)	0	0	0
Interlevel metal insulator—effective dielectric constant (κ)	1.5	<1.5	<1.5

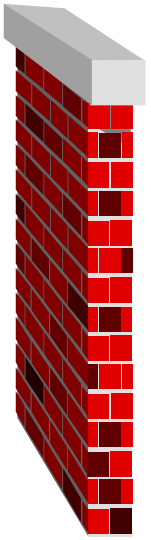
Solutions Exist | Solutions Being Pursued | No Known Solutions

DRAM Interconnect technology

What is a Red Brick Wall?



- The Red Brick Wall is not used in the ITRS
- The concept has been introduced in presentations to separate and to highlight a region in a table that is mostly “RED” beyond a certain year
- The Red Brick Wall is a good instrument to highlight problem areas

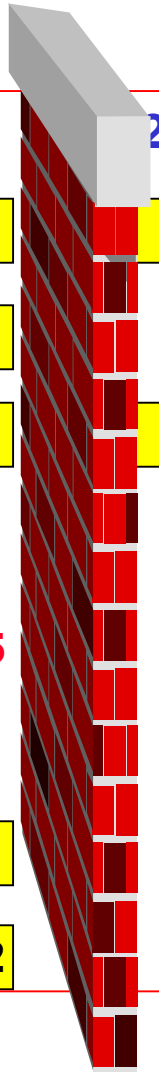


Approaching a "Red Brick Wall"

1999 Results

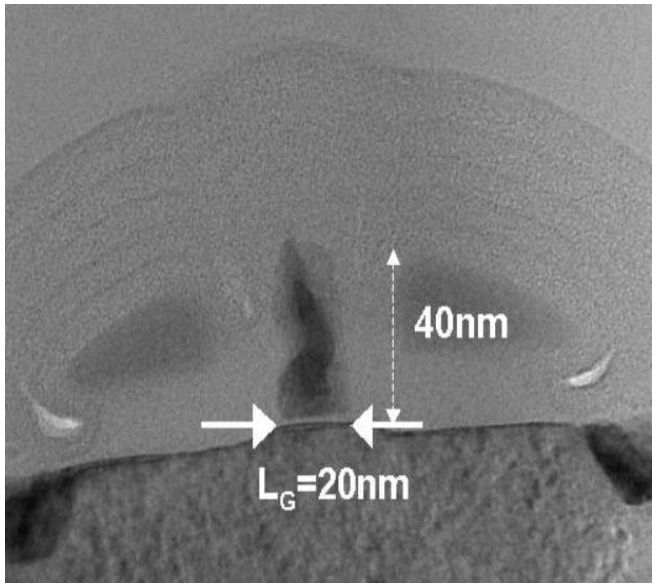
Challenges/Opportunities for Semiconductor R&D

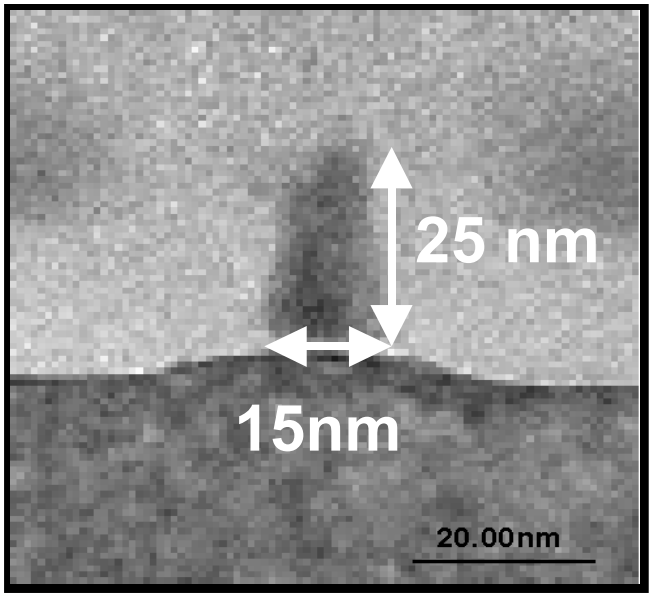
Year of Production:	1999	2002	2005	2008	2011	2014
DRAM Half-Pitch [nm]:	180	130	100	70	50	35
Overlay Accuracy [nm]:	65	45	35	25	20	15
MPU Gate Length [nm]:	140	85-90	65	45	30-32	20-22
CD Control [nm]:	14	9	6	4	3	2
T_{OX} (equivalent) [nm]:	1.9-2.5	1.5-1.9	1.0-1.5	0.8-1.2	0.6-0.8	0.5-0.6
Junction Depth [nm]:	42-70	25-43	20-33	16-26	11-19	8-13
Metal Cladding [nm]:	17	13	10	0	0	0
Inter-Metal Dielectric K:	3.5-4.0	2.7-3.5	1.6-2.2	1.5	<1.5	<1.5

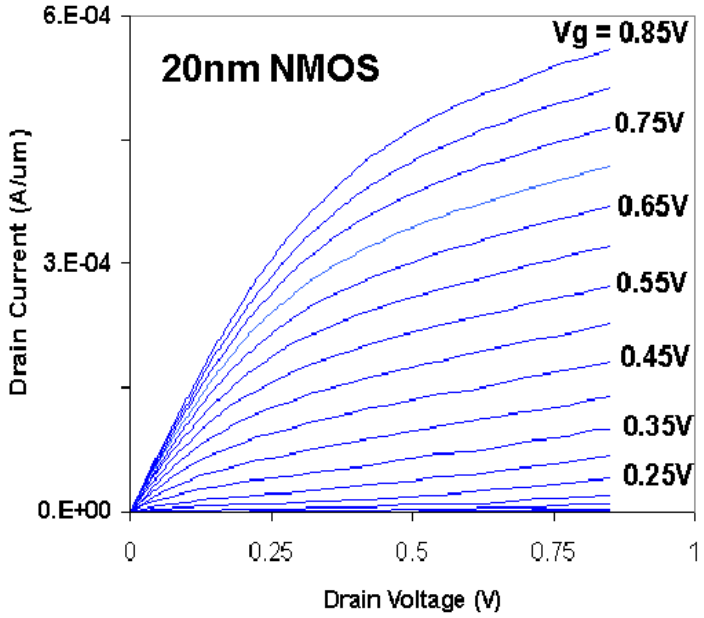


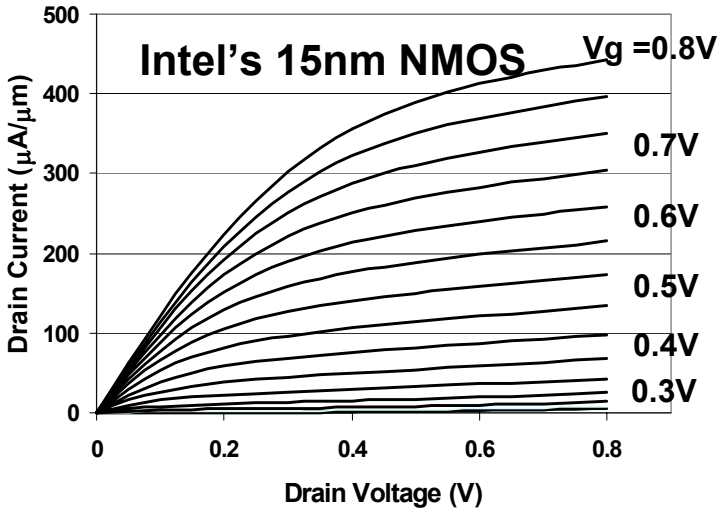
Who is afraid of "The Red Brick Wall???"

Attacking the Red Brick Wall







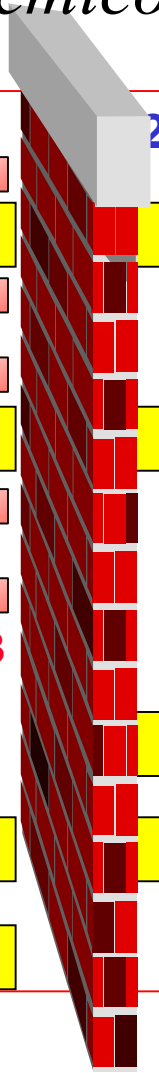


"Red Brick Wall" becoming permeable

2001 Results

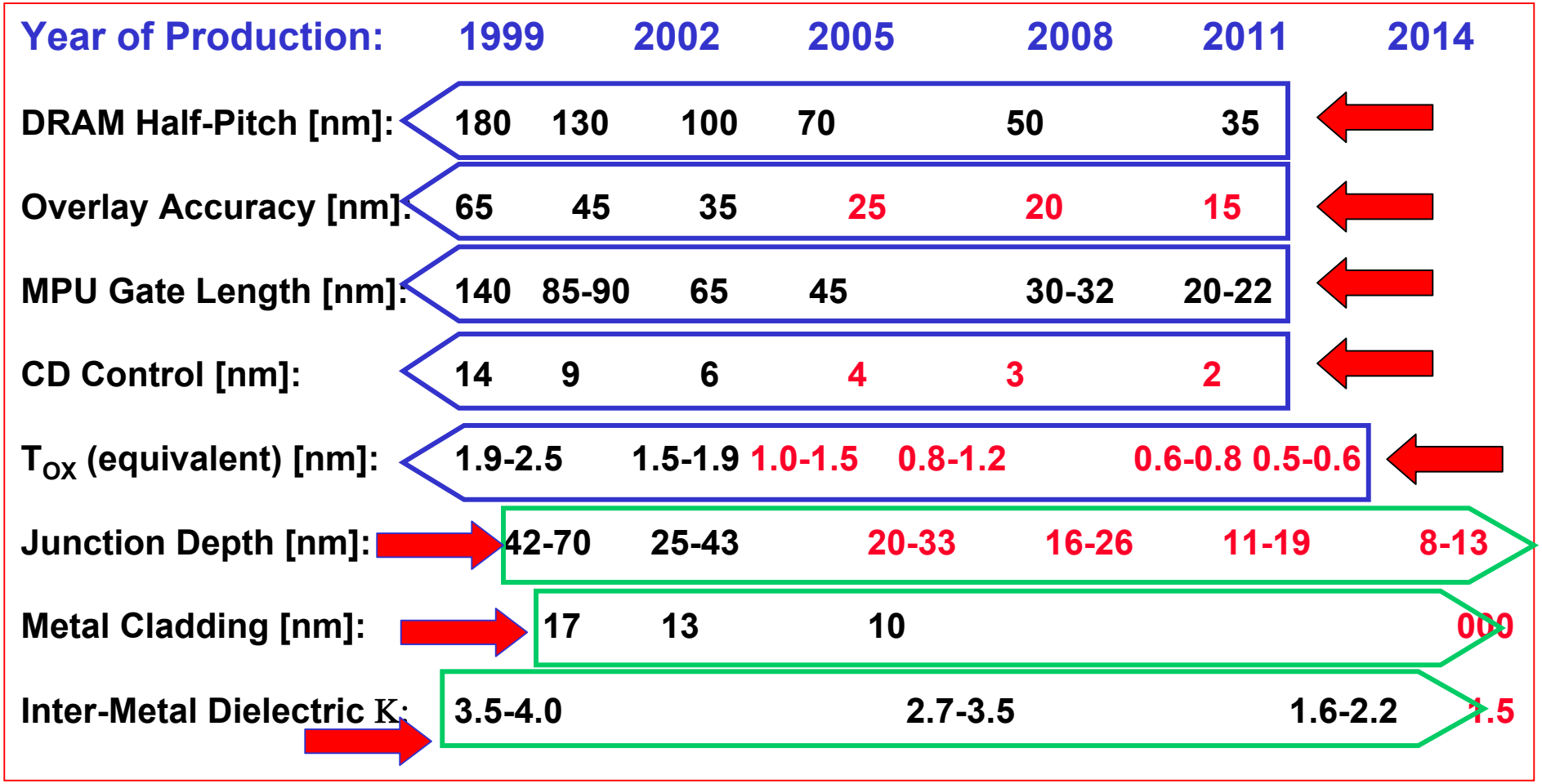
Challenges/Opportunities for Semiconductor R&D

Year of Production:	2001	2003	2005	2007	2010	2016
DRAM Half-Pitch [nm]:	130	100	80	65	45	22
Overlay Accuracy [nm]:	46	35	28	23	18	9
MPU Gate Length [nm]:	90	65	45	35	25	13
CD Control [nm]:	8	5.5	3.9	3.1	2.2	1.1
T_{OX} (equivalent) [nm]:	1.3-1.6	1.1-1.6	0.8-1.3	0.6-1.1	0.5-0.8	0.4-0.5
Junction Depth [nm]:	48-95	33-66	24-47	18-37	13-26	7-13
Metal Cladding [nm]:	16	12	9	7	5	2.5
Inter-Metal Dielectric K:	3.0-3.6	3.0-3.6	2.6-3.1	2.3-2.7	2.1	1.8

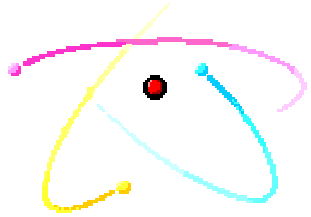


Roadmap Acceleration and Deceleration

2001 versus 1999 Results



CLASSICAL CMOS And BEYOND

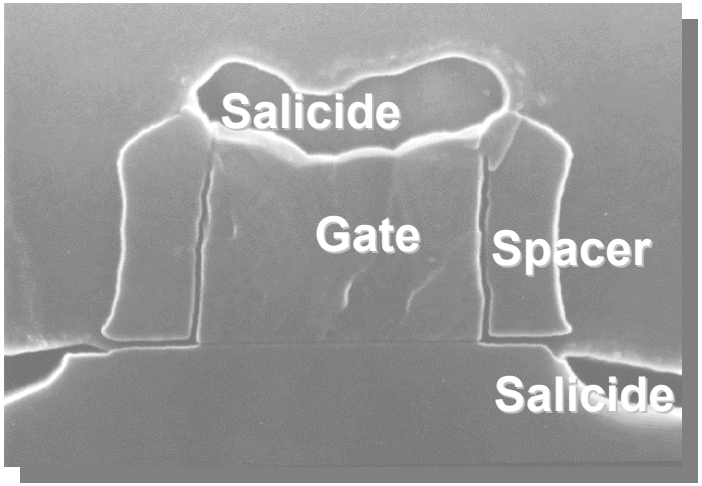


MOS Transistor Scaling
(1974 to present)

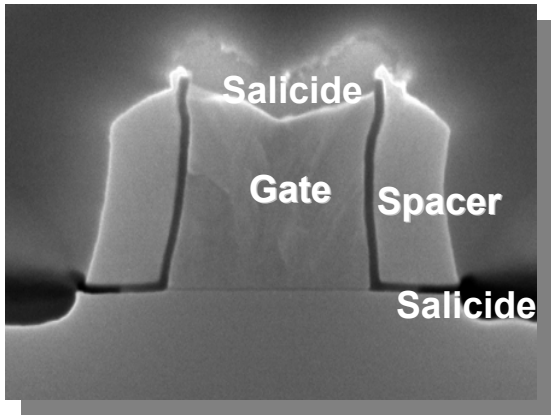
S=0.7

[0.5x per 2 nodes]

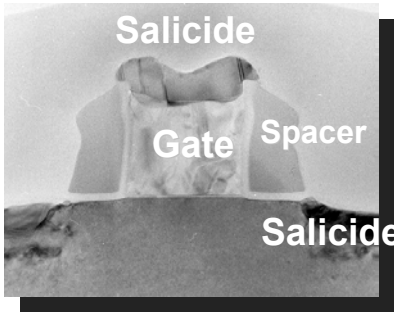
The Incredible Shrinking Silicon Technology



0.35μ

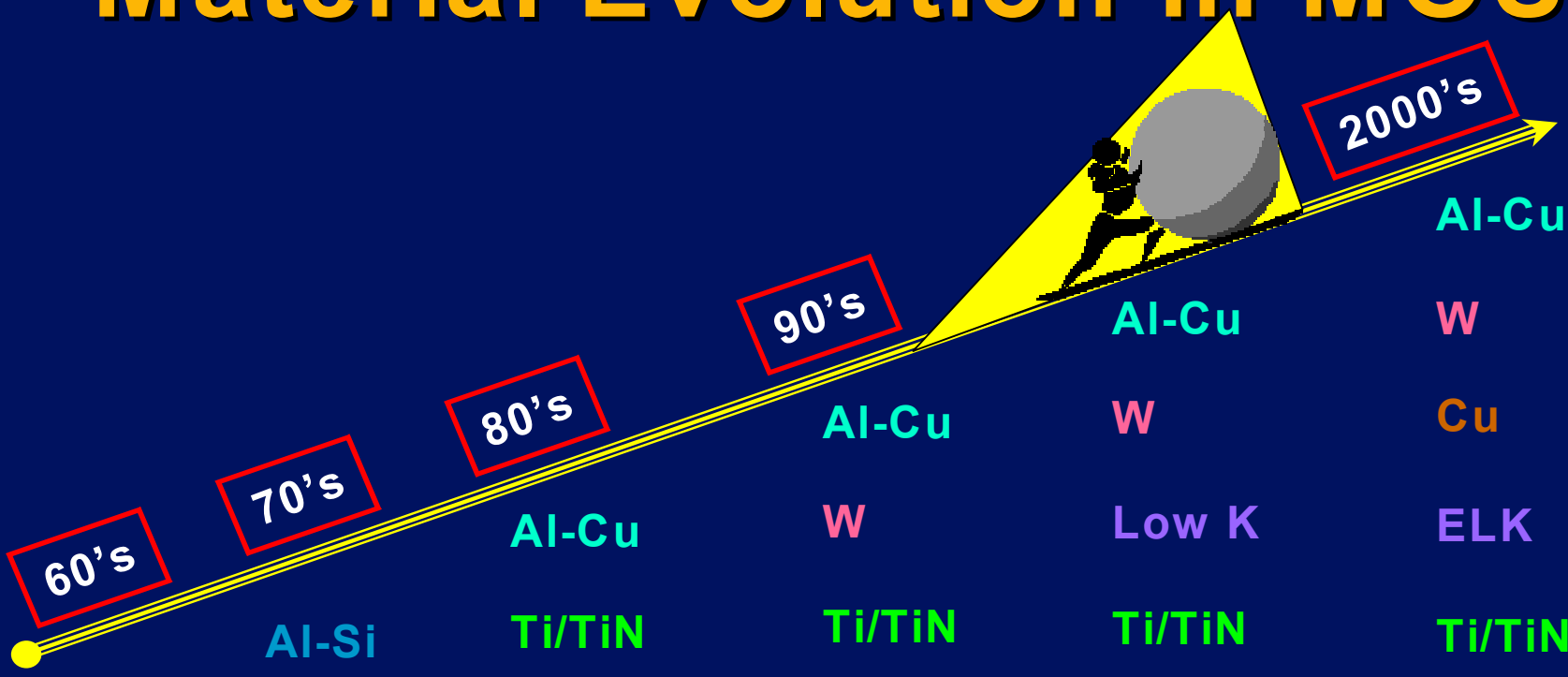


0.25μ



0.18μ

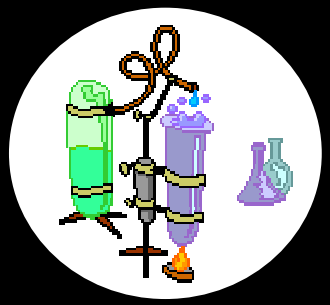
Material Evolution in MOS



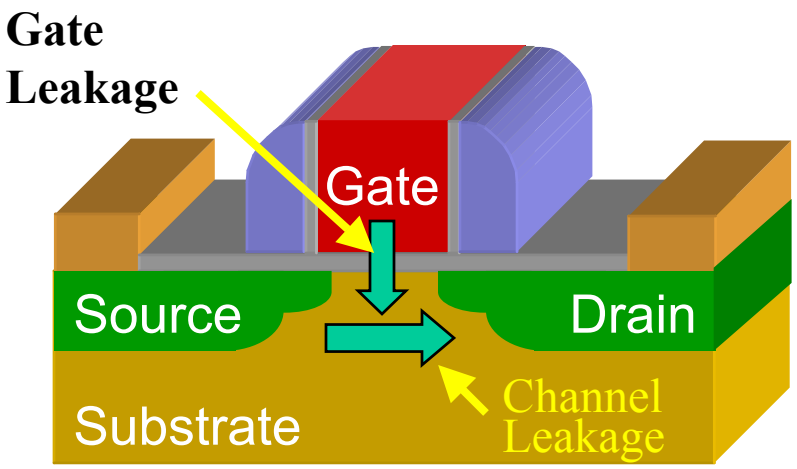
Material Evolution in MOS

Material Additions | Material Replacements

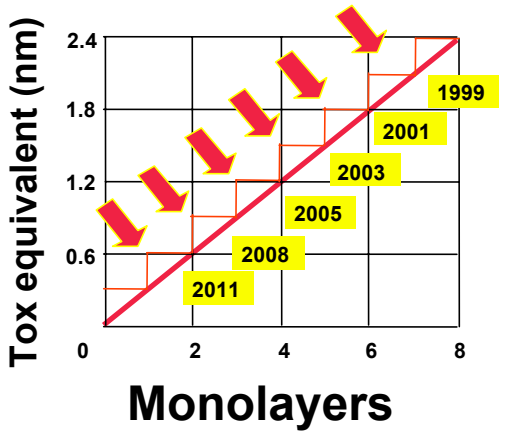
70's	90's	2000-2010
	Al-Cu	Cu/New
	SiO2	New/Voids
	W	
Al-Si	Ti/TiN	New
Poly	TiSi2/Poly	New
SiO2	SiO2	New



Bulk-Si MOSFET



Gate Dielectric Scaling

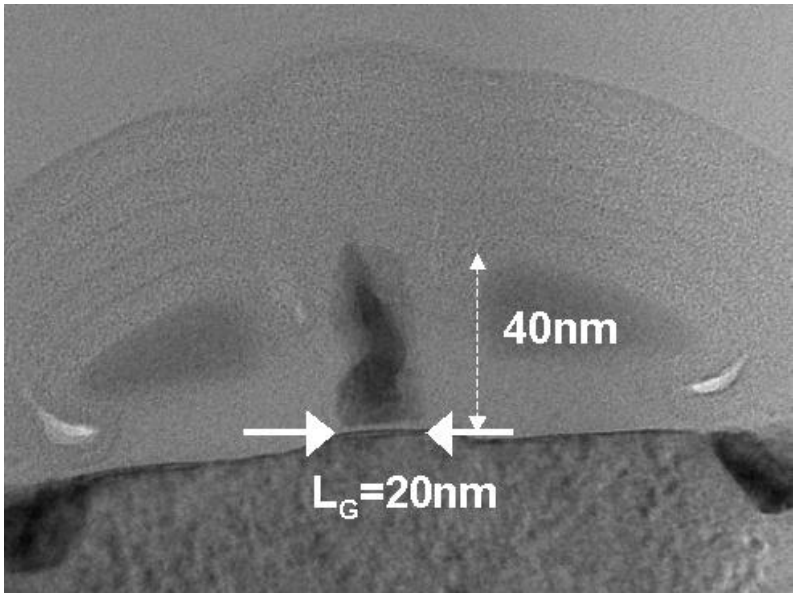


12

Primary barriers to MOSFET scaling are:

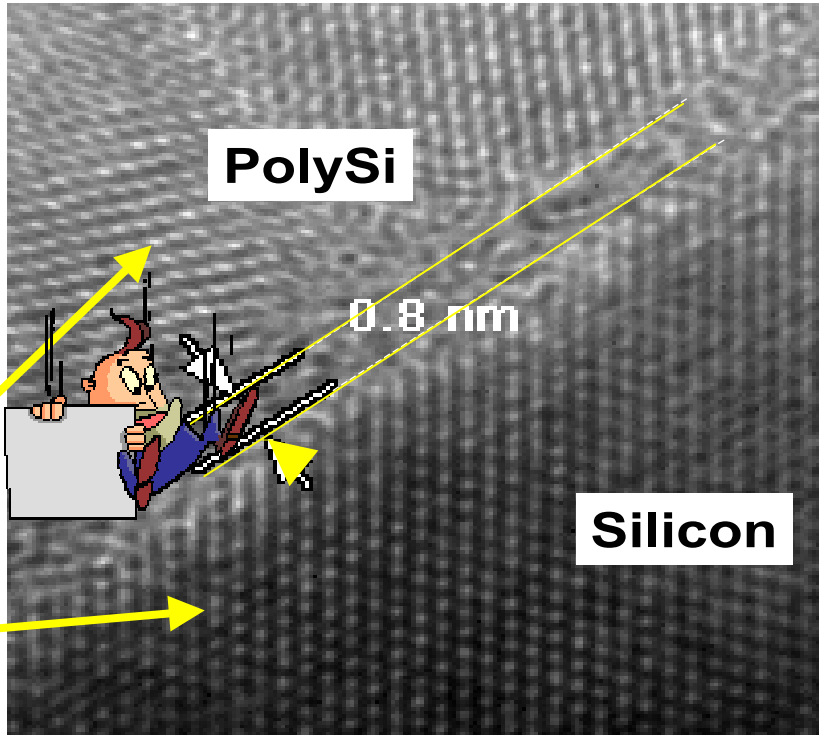
- High I_{on}/I_{off} ratio (I_{off} = Channel leakage current)
- Low Standby leakage current (Gate + Channel leakage)
  - Low channel leakage current (Electrostatic scaling)
  - Low gate leakage current

Is There Any Oxide Left?



20 nanometer transistor

Gate oxide less than 3 atomic layers thick



Atomic structures

Bulk CMOS Scaling Challenges

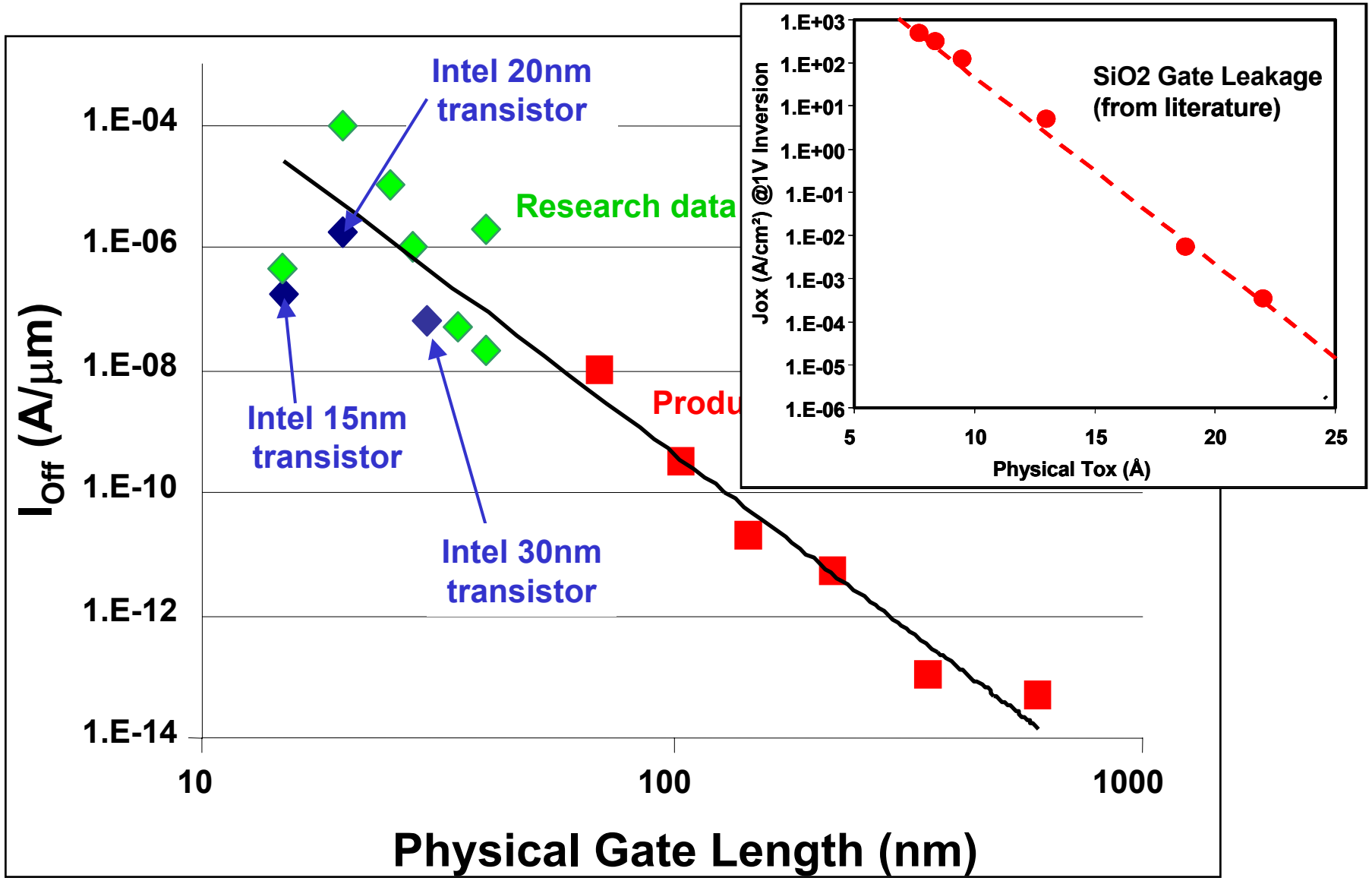
Table 2a High Performance Logic Technology Requirements—2001 ITRS

CALENDAR YEAR	2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
TECHNOLOGY NODE	130NM			90NM			65NM	45NM	32NM	22NM
MPU GATE LENGTH	65	53	45	37	32	30	25	18	13	9
Gate Dielectric Equivalent Oxide Thickness (EOT) (nm) [1]	1.45	1.35	1.35	1.15	1.05	0.95	0.85	0.65	0.50	0.45
Electrical Thickness Adjustment Factor (Gate Depletion and Quantum Effects) (nm) [2]	0.8	0.8	0.8	0.8	0.8	0.8	0.5	0.5	0.5	0.5
Tox Electrical Equivalent (nm) [3]	2.25	2.15	2.15	1.95	1.85	1.75	1.35	1.15	1.00	0.95
Vdd (V) [4]	1.2	1.2	1.1	1.0	0.9	0.9	0.8	0.6	0.5	0.4
Sub-Threshold I-off @25°C (uA/um) [5]	0.01	0.03	0.07	0.1	0.3	0.7	1	3	7	10
Id-NMOS @Vdd (uA/um) [6]	926	1001	924	905	878	961	1076	1218	1523	1465
Required "Technology Improvement" (SOI/Low-Temp/High-mobility) [7]	0%	0%	0%	0%	0%	0%	0%	30%	70%	100%
Rsd Percent of Ideal Channel Resistance (Vdd/IdNMOS with no RSD) [8]	16%	16%	17%	18%	19%	19%	20%	25%	30%	35%
Parasitic Capacitance Percent of Cgate [9]	19%	22%	25%	27%	29%	29%	27%	31%	35%	42%
Intrinsic Frequency (1/Tau) (GHz) [10]	624	764	873	1013	1166	1282	1531	2603	4424	6460
Relative Device Performance [11]	1.0	1.2	1.4	1.6	1.9	2.1	2.5	4.2	7.1	10.3
Relative Device Switching Energy [12]	1.0	0.72	0.45	0.29	0.19	0.17	0.12	0.04	0.02	0.01

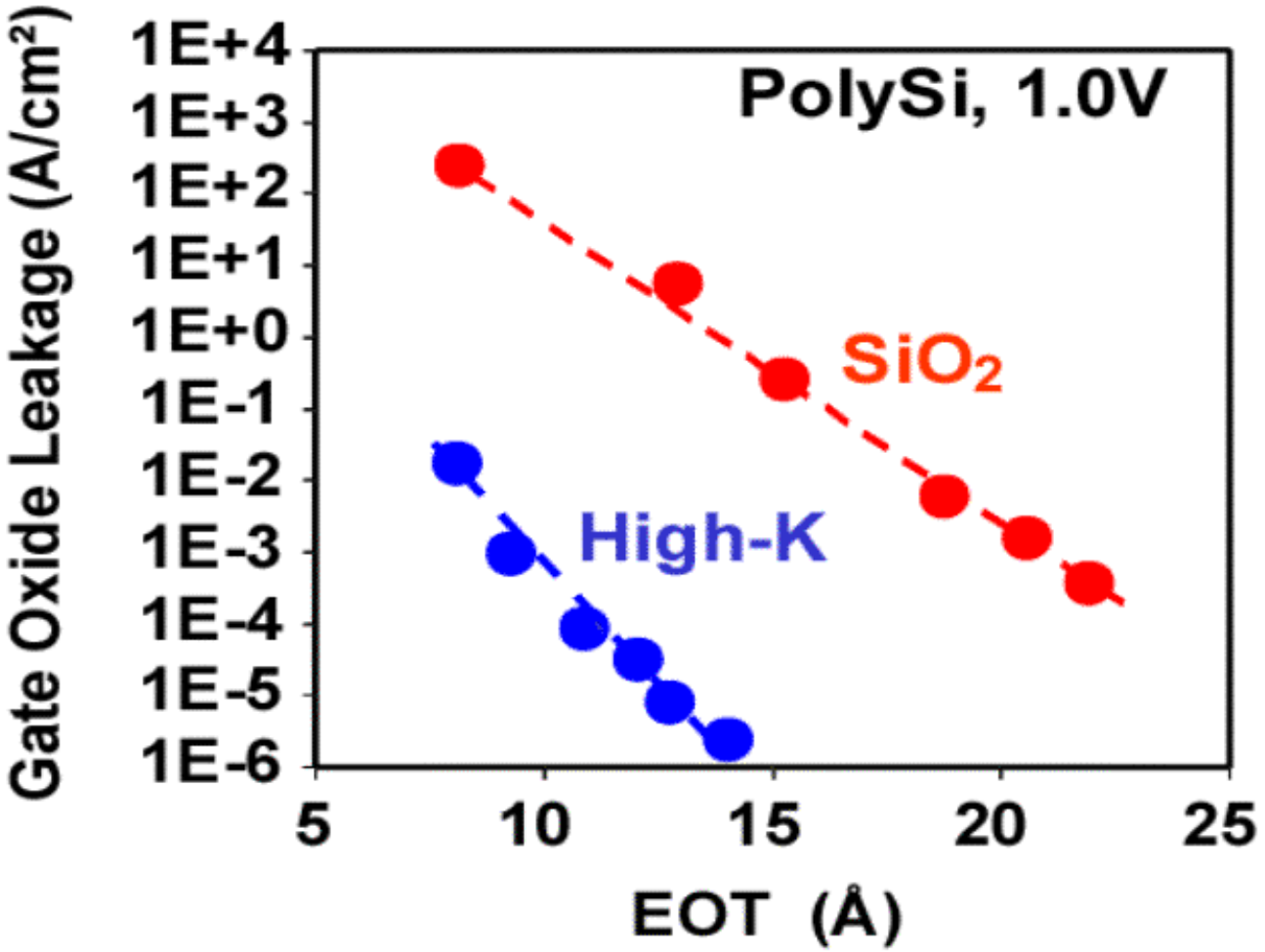
M2 S2

P.Gargini

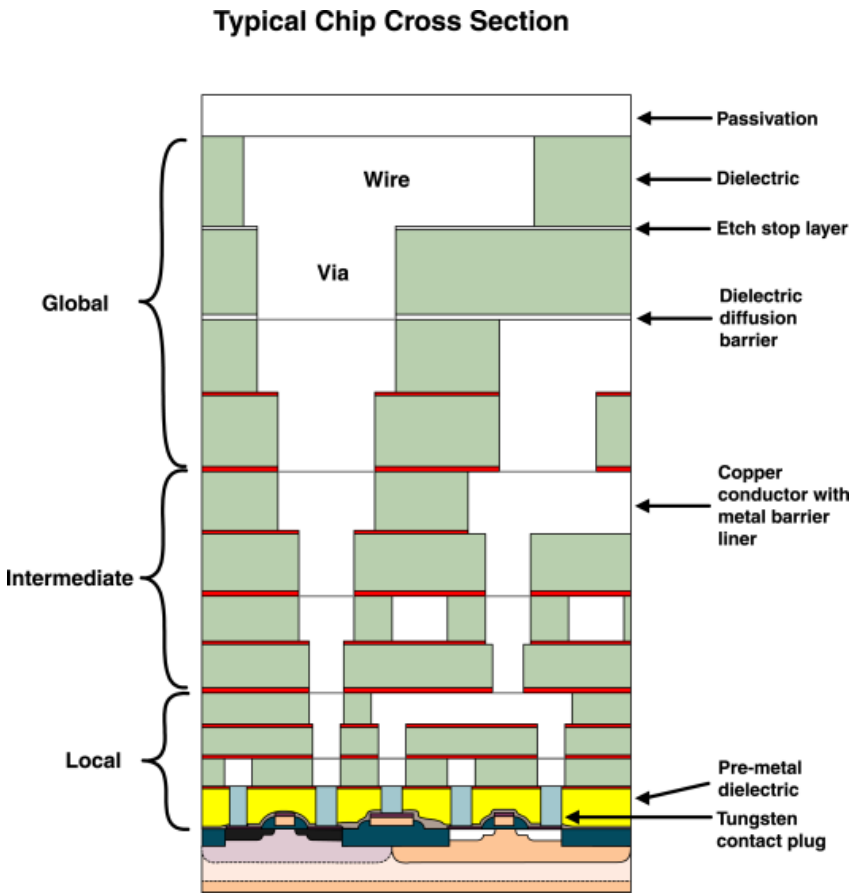
…but Leakage Keeps Increasing



High-K Dielectrics



Interconnect Grand Challenges



Near Term (2001-2007)

Enhancing Performance

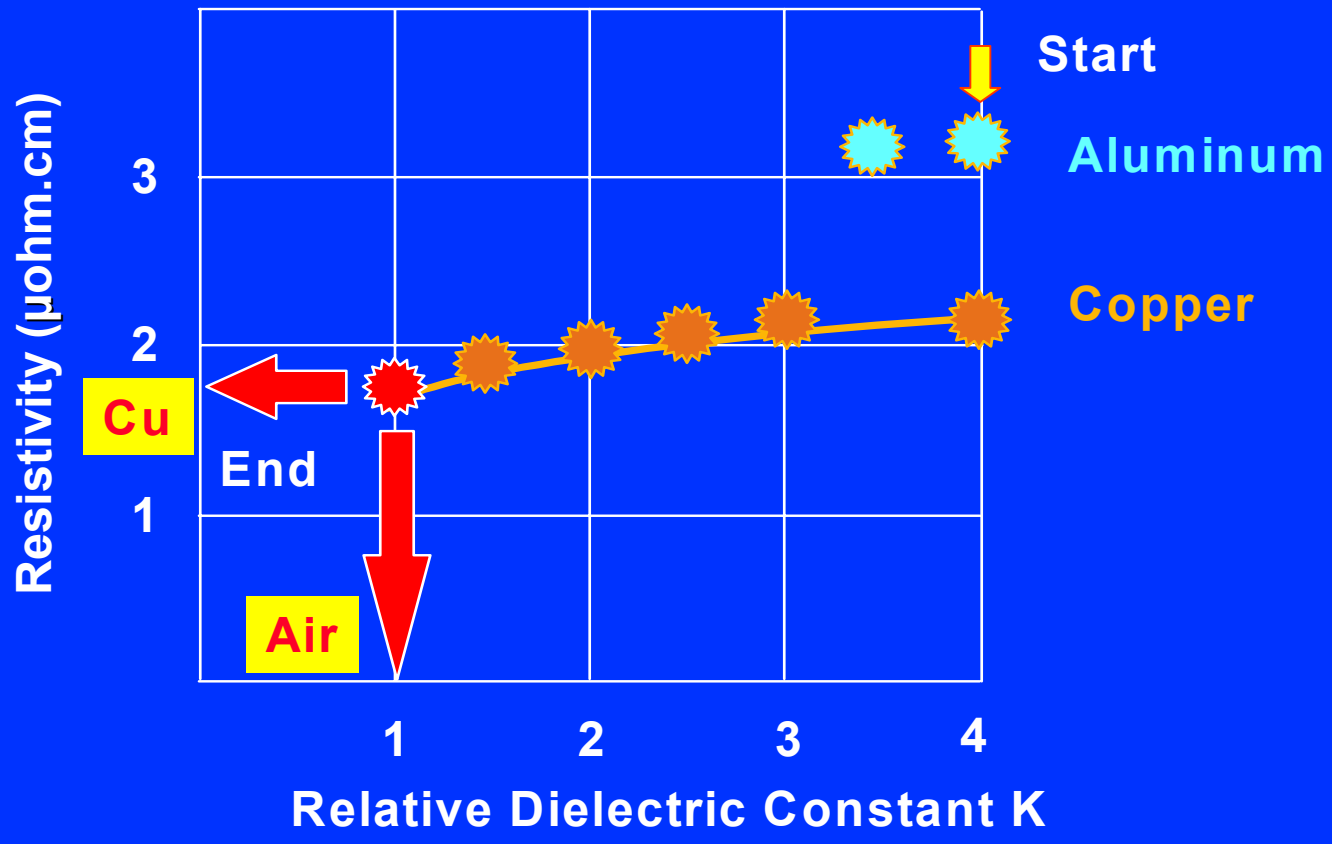
- **Introduction of New Materials :**
  - **High Conductivity and Low k Dielectric**
- **Integration of New Processes and Structures :**
  - **High Complexity**

Long Term (2008-2016)

Enhancing Performance

- **Identify Solutions which address Global Wiring Scaling:**
  - **Beyond Copper and Low k**
  - **Material Innovation to accelerate Design, Package and Interconnect**

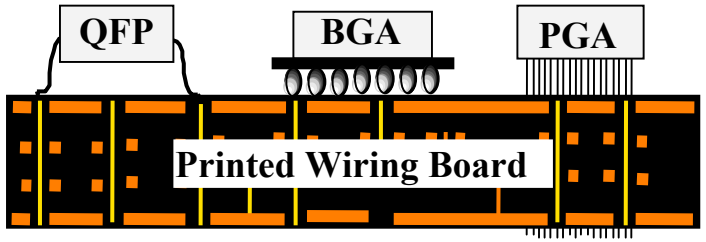
Interconnect and Dielectric Materials



Assembly & PKG Grand Challenges

Chip

Package

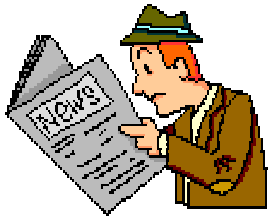


Near Term (2001-2007)

Cost-effective Manufacturing

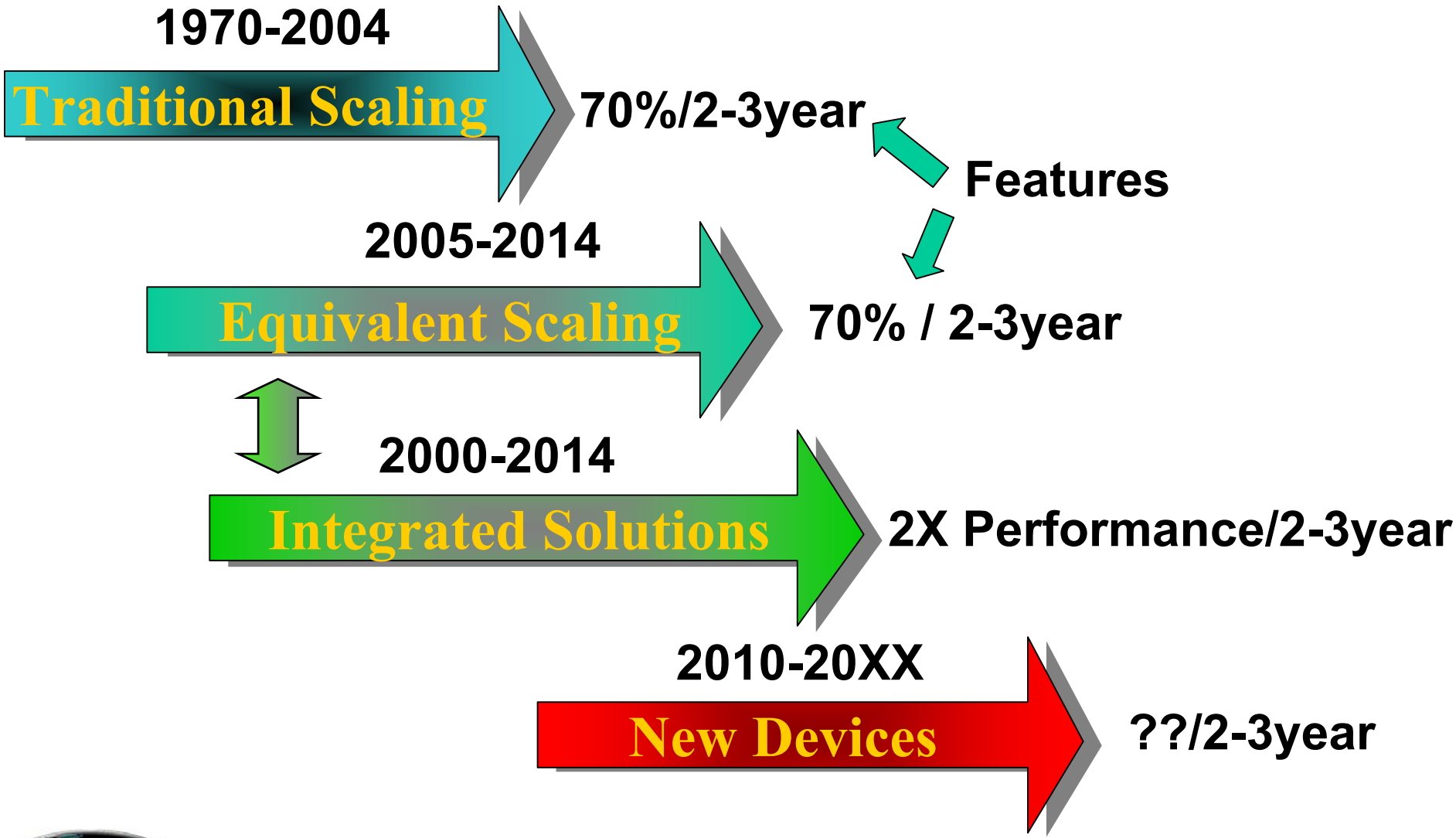
■ Coordinated Design Tools and Simulators :

- Mix Signal Co-design and Simulation
- Transient Thermal Analysis Tool
- Thermal Mechanical Analysis Tool
- Electrical Analysis Tool
  - Power Disturbs
  - EMI
  - High Frequency / Current and Lower Voltage Switching

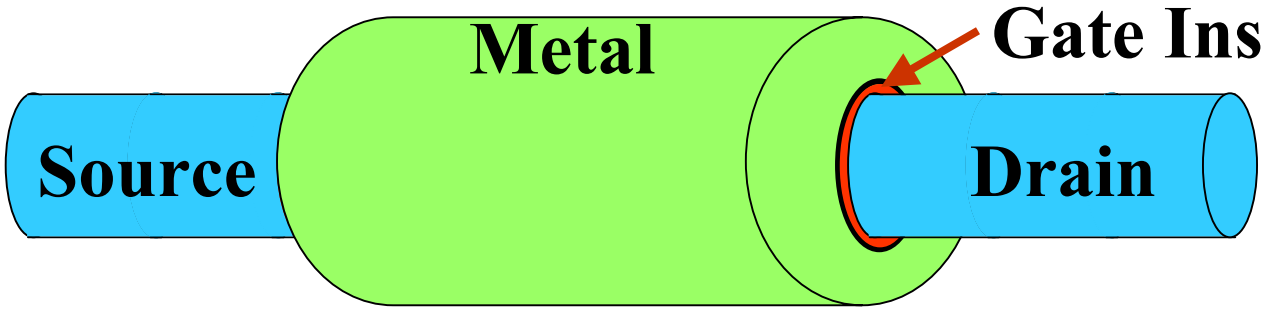


Emerging Research Devices

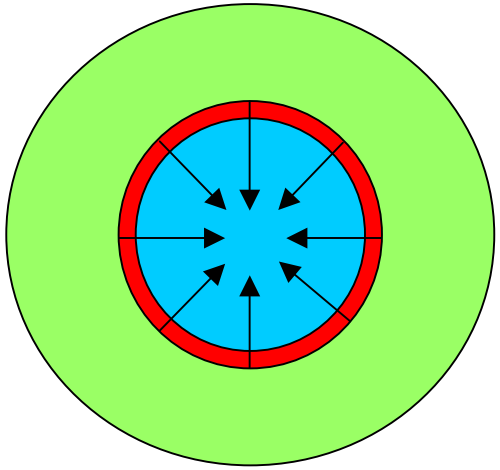
CMOS Future Directions



The Ideal MOS Transistor



Fully Surrounding Metal Electrode



Fully Enclosed, Depleted Semiconductor

High-K Gate Insulator

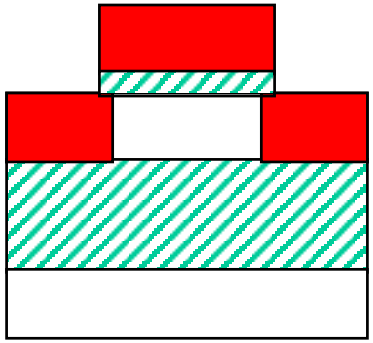
Band Engineered Semiconductor

Low Resistance Source/Drain

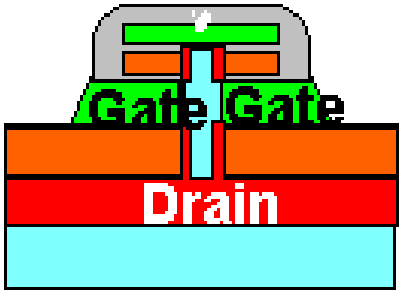
Emerging Research Devices
Pursuing CMOS Scaling to the End

- **Bulk CMOS**
  - **Conventional bulk (SiO2, poly gate, etc..)**
  - **Introduction of new materials (high-K gate, metal gate electrode,high mobility channel, etc.)**
- **Non Classical CMOS Structures**
  - **Ultra thin channel (SOI)**
  - **Channel engineered structures**
  - **Double gate MOSFETs**

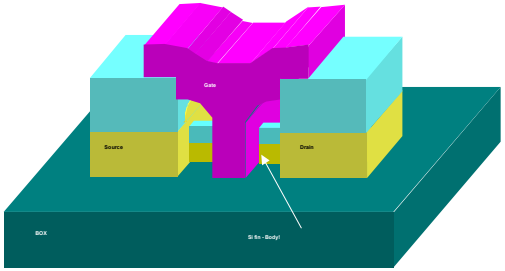
2001 ITRS
New Transistor Definitions



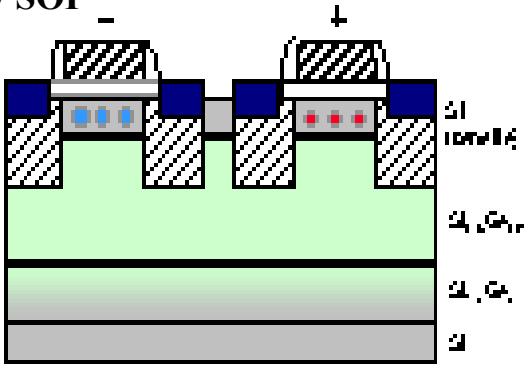
Ultra-Thin Body SOI



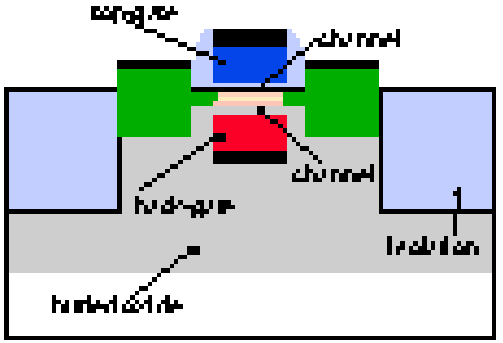
Vertical Transistor



FinFET



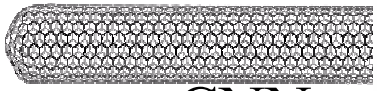
Band Engineered Transistor



Double Gate Transistor

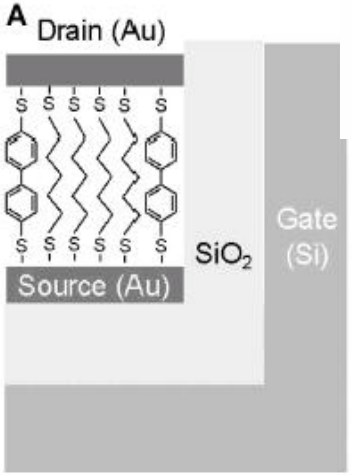
… and beyond

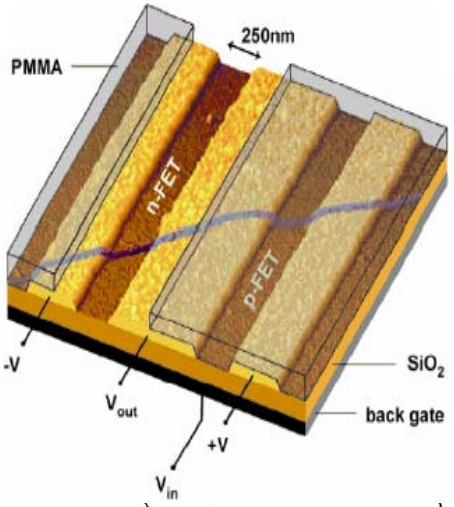
Nanotube

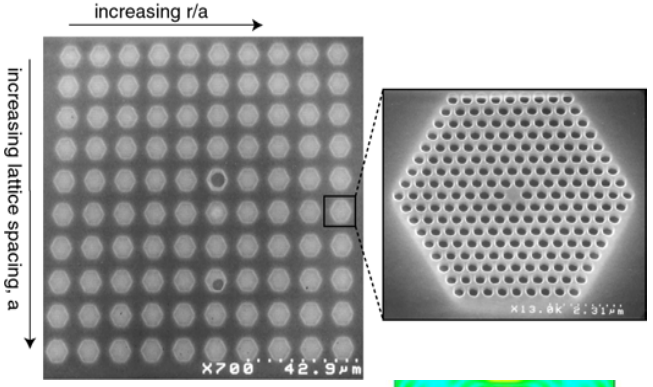


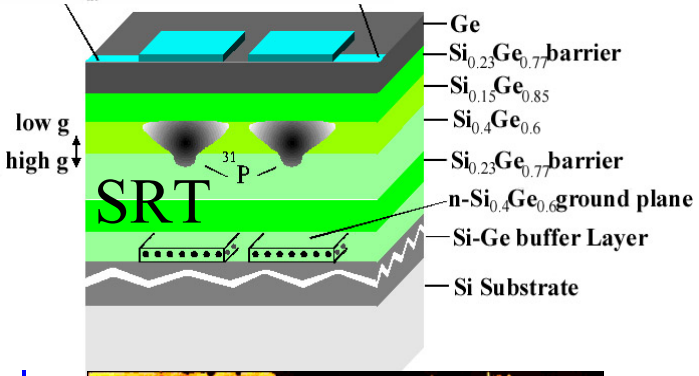
CNN

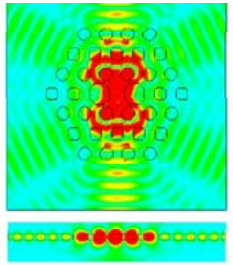
Molecular





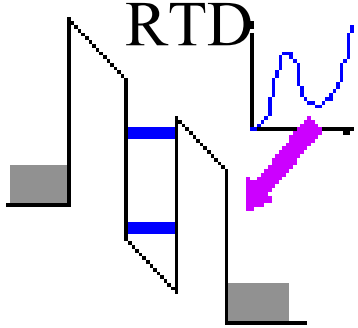


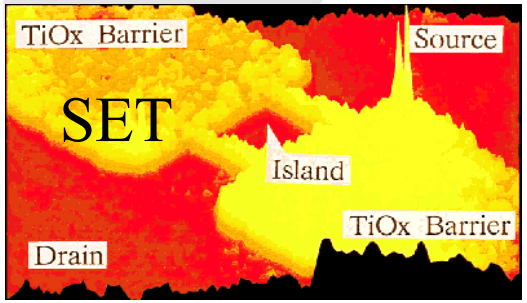


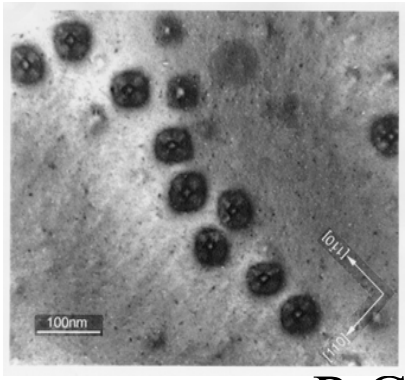


QD

RTD



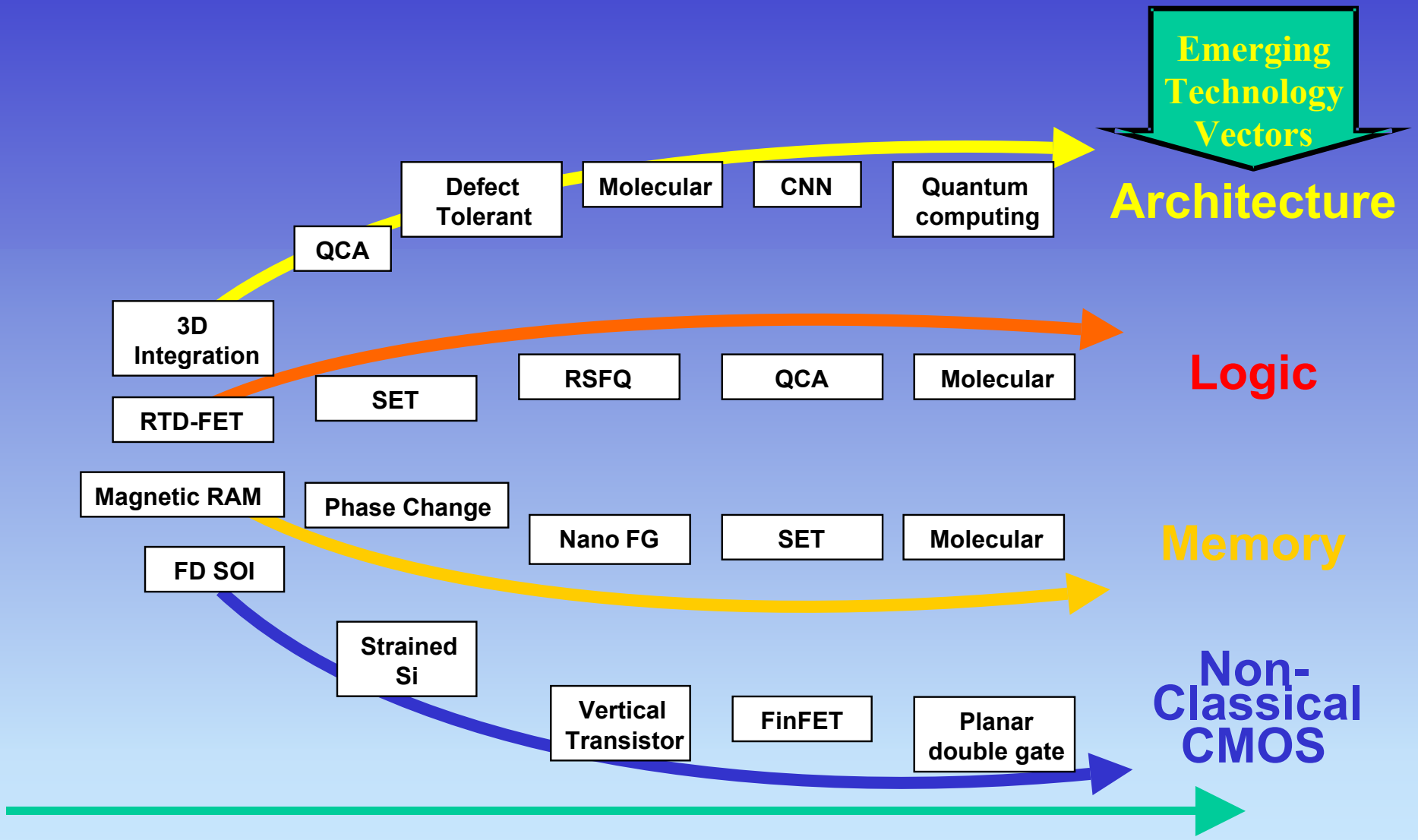




M2 S2

P.Gargini

Emerging Technology Sequence



Conclusions

- **The ITRS** has become a common **reference document** for the **Semiconductor Community**
- **CMOS** will **remain** the device of choice for the foreseeable future **(>10yrs)**
- Introduction of **Non-classical** CMOS in manufacturing will occur within this decade **(~5years)**
- Many **new materials** will be necessary->**Back to basics**
- Design, Silicon Process, Package and System interaction will continue to increase-> Need **integrated design** methodology
- **Innovation in:** Architecture, Logic, Memory and Devices is marking the ***Renaissance*** of the Semiconductor Industry
- **Economical** challenges are **exceeding** the resources of any individual company or consortium-> Cooperation is a must
- **"Red Brick Walls"** represent an efficient way of identifying and attacking industry–wide challenges


SUPPORT THE ITRS!!!!
IT IS A MATERIAL WORLD!!!!